PSE Conf. Suite Regression

May 27 2022 6:52 PM

Port Count..... 4
Loop Count..... 1
PSE Tested: Sample Type-1 PSE

Sifos Technologies

802.3at Conformance Report

version 5.3.00
report version 5.3.0a

Test Mode: 15.4 Watt
Sifos Interop Index*: 99%
Error Log: None

Chassis ID: 192.168.221.141	PSA-3000 Ports											
TestLoop: 1	11-1	11-2	12-1	12-2	UNITS	Min	Max	Average	Low Limit	P/F	High Limit	P/F
Test: det_v												
Open_Circuit_Det_Voc=	4.58	4.95	4.78	4.9	V	4.58	4.95	4.8	2.8	Pass	30	Pass
Peak_Det_Vvalid=	8.4	8.69	8.49	8.55	V	8.4	8.69	8.5	3.8	Pass	10	Pass
Min_Det_Vvalid=	4.69	4.9	4.77	4.8	V	4.69	4.9	4.8	2.8	Pass	9	Pass
Det_Volt_Step_dVtest=	3.71	3.79	3.72	3.75	V	3.71	3.79	3.7	1	Pass	7.2	Pass
Detection_Slew=	0	0	0	0	V/usec	0	0	0	0	Pass	0.1	Pass
Good_Sig_Det_Pulse=	1	1	1	1	edges	1	1	1	1	Pass	9	Pass
Backoff_Voltage=	0.1	0.1	0.1	0.1	V	0.1	0.1	0.1	0	Pass	9	Pass
Non_802_Discr_?=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Detect_Strategy=	1	1	1	1	****	1	1	1	0	Pass	2	Pass
Test: det_i												
Init_Current_Isc=	0.36	0.38	0.37	0.37	mA	0.36	0.38	0.37	0	Pass	5	Pass
Det_Current_Isc=	0.33	0.35	0.34	0.34	mA	0.33	0.35	0.34	0	Pass	5	Pass
Test: det_range												
Rgood_Max=	29	28	28	28	Kohm	28	29	28.3	26	Pass	32	Pass
Rgood_Min=	17	16	17	16	Kohm	16	17	16.5	16	Pass	19	Pass
Rmid_det=	29	28	28	28	Kohm	28	29	28.3	26	Pass	33	Pass
Cgood_Max=	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Rbad_Cbad_Stat=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Test: det_time												
Backoff_Time_Tdbo=	563	453	461	461	msec	453	563	484.5	-1	Pass	1500	Pass
Eff_Backoff_Tdbo_eff=	563	453	461	461	msec	453	563	484.5	-1	Pass	1500	Pass
Backoff_Type=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Detection_Time_Tdet=	141	141	141	141	msec	141	141	141	5	Pass	500	Pass
Total_Det_Time=	377	379	381	381	msec	377	381	379.5	5	Pass	1000	Pass
Test: det_rsource												
PSE_Detect_Source=	1	1	1	1	****	1	1	1	0	Pass	1	Pass
Output_Impedance_Zout=	**44.9**	45.5	45.4	**44.1**	Kohm	44.1	45.5	45	45	**Info**	2000	Pass
Test: class_v												
Vclass_Max=	17.6	17.8	17.7	17.6	V	17.6	17.8	17.7	15.5	Pass	20.5	Pass
Vclass_Min=	16.9	17.2	17.2	17	V	16.9	17.2	17.1	15.5	Pass	20.5	Pass
Test: class_time												
Class_0_Count=	1	1	1	1	****	1	1	1	0	Pass	1	Pass
Class_4_Count=	1	1	1	1	****	1	1	1	0	Pass	1	Pass
Class_Time_Tpdc=	30	30	30.4	30	msec	30	30.4	30.1	5.6	Pass	75	Pass
Test: class_err												
Class_lim=	70	71	65	65	mA	65	71	68	51	Pass	100	Pass
Pwr_Cl_lim=	1	1	1	1	****	1	1	1	0	Pass	1	Pass
Pwr_Cl_55=	1	1	1	1	****	1	1	1	0	Pass	1	Pass
Test: pwrup_time												
Power-On_Trise_c0=	63	62	75	74	usec	62	75	69	15	Pass	50000	Pass
Power-On_Tpon_c0=	58.6	60.6	60.6	60.6	msec	58.6	60.6	60.1	0	Pass	400	Pass
Test: pwrup_inrush												
Init_Iinrush=	413.25	416	417.5	417	mA	413.25	417.5	415.9	400	Pass	450	Pass
Max_Iinrush_c0=	413	415.75	417.88	417	mA	413	417.88	415.9	400	Pass	450	Pass
Min_Iinrush=	412.63	415.38	416.75	416.25	mA	412.63	416.75	415.3	400	Pass	450	Pass
Tinrush=	64.6	64.6	63.9	64.6	msec	63.9	64.6	64.4	50	Pass	75	Pass
Inrush_45m=	47.2	47.3	47.1	47.2	V	47.1	47.3	47.2	44	Pass	57	Pass
Inrush_Voltage=	31.1	31.2	35.1	34.8	V	31.1	35.1	33.1	30	Pass	57	Pass
Inrush_Strategy_c0=	0	0	1	1	****	0	1	1	0	Pass	1	Pass
Test: pwron_v												
Vport_min=	46.2	46.5	46.3	46.4	V	46.2	46.5	46.4	44	Pass	57	Pass
Vport_max=	47.5	47.6	47.4	47.5	V	47.4	47.6	47.5	44	Pass	57	Pass
Vport_ripple=	2	2	3	3	mVpp	2	3	2.5	0	Pass	500	Pass
Vport_noise=	4	5	7	8	mVpp	4	8	6	0	Pass	200	Pass
Vtrans_min=	46	46.4	46.1	46.2	V	46	46.4	46.2	44	Pass	57	Pass
Vtrans_max=	47.7	47.6	47.4	47.6	V	47.4	47.7	47.6	44	Pass	57	Pass
Test: pwron_pwrcap												
Pcon_c0=	15.9	16	15.9	15.9	W	15.9	16	15.9	14.2	Pass	22.7	Pass
Icon_%_c0=	105.7	106.2	105.7	105.9	%	105.7	106.2	105.9	100	Pass	9999	Pass
Pcon_c1=	4.3	4.3	4.3	4.3	W	4.3	4.3	4.3	3.9	Pass	22.7	Pass
Icon_%_c1=	107.8	108.1	107.6	107.8	%	107.6	108.1	107.8	100	Pass	9999	Pass
Pcon_c2=	7.6	7.6	7.6	7.6	W	7.6	7.6	7.6	6.8	Pass	22.7	Pass
Icon_%_c2=	109.9	110.3	109.5	110.1	%	109.5	110.3	110	100	Pass	9999	Pass
Pcon_c3=	15.9	16	15.9	15.9	W	15.9	16	15.9	14.2	Pass	22.7	Pass
Icon_%_c3=	105.7	106.2	105.7	105.9	%	105.7	106.2	105.9	100	Pass	9999	Pass
Pcon_c4=	15.9	16	15.9	15.9	W	15.9	16	15.9	14.2	Pass	22.7	Pass
Icon_%_c4=	105.7	106.2	105.7	105.9	%	105.7	106.2	105.9	100	Pass	9999	Pass
Test: pwron_maxi												
Ilim_Peak_1=	71.8	73	72.3	71.3	mA	71.3	73	72.1	0	Pass	1750	Pass
Ilim_Min_1=	402	402.3	401.4	401.9	mA	401.4	402.3	401.9	400	Pass	1750	Pass
Tlim_1=	64.5	64.1	64.1	64.5	msec	64.1	64.5	64.3	50	Pass	75	Pass
Vlim_1=	45.8	46.1	45.9	46	V	45.8	46.1	46	44	Pass	57	Pass
Ilim_Max_1=	413.3	416.3	418.5	417.8	mA	413.3	418.5	416.5	400	Pass	1750	Pass
Ktran_lo_1=	-1	-1	-1	-1	%	-1	-1	-1	-1	Pass	-1	Pass
Test: pwron_overld												
%Ipeak_1=	111	113.9	113.7	113.8	%	111	113.9	113.1	100	Pass	125	Pass
Vport_Ipeak_1=	46	46.3	46	46.1	V	46	46.3	46.1	44	Pass	57	Pass
Vport_5%DC_1=	46	46.3	46	46.1	V	46	46.3	46.1	44	Pass	57	Pass
Test: mps_ac_pwrdn												
Power_Down_Time_Tmpdo=	**295**	300	**295**	**295**	msec	295	300	296	300	**Fail**	400	Pass
DC_Max_Load_Imin1=	0	0	0	0	mA	0	0	0	0	Pass	0	Pass
Test: mps_ac_vf												
AC_MPS_V_open=	4.7	4.7	4.8	4.8	Vpk	4.7	4.8	4.8	1.9	Pass	5.7	Pass
AC_MPS_V_open%=	9.7	9.6	9.8	9.8	%Vport	9.6	9.8	9.7	3.25	Pass	10	Pass
AC_MPS_Frequency=	25	28	25	23	Hz	23	28	25	0	Pass	500	Pass
Slew_Rate=	0	0	0	0	V/usec	0	0	0	0	Pass	0.1	Pass
Source_Current_Isac=	0.001	0.001	0.001	0.001	mA	0.001	0.001	0	0	Pass	5	Pass
Test: mps_ac_voff												
Peak_AC_MPS_V_open1=	4.6	5	4.8	4.8	Vpk	4.6	5	4.8	0	Pass	30	Pass
Peak_Disconnect_Vport=	52.8	52.8	52.7	52.8	V	52.7	52.8	52.8	0	Pass	60	Pass
Test: pwrdn_overld												
Icut_1=	355.8	355.8	355.8	355.8	mA	355.8	355.8	355.8	-1	Pass	1750	Pass
Tcut_1=	63.1	63.7	64	65	msec	63.1	65	64	50	Pass	9999	Pass
Isoft_1=	-1	-1	-1	-1	mA	-1	-1	-1	-1	Pass	399	Pass
Tsoft_1=	-1	-1	-1	-1	msec	-1	-1	-1	-1	Pass	2000	Pass
Test: pwrdn_time												
Turn-Off_Time_Toff=	12.3	12.1	12.1	12.6	msec	12.1	12.6	12.3	0	Pass	500	Pass
Output_Cap_Cout=	0.0982	0.0982	0.0961	0.1046	uF	0.0961	0.1046	0.1	-1	Pass	0.52	Pass
Output_Load_Rp=	53.6	52.4	53.7	50.8	Kohm	50.8	53.7	53	45	Pass	50000	Pass
Test: pwrdn_v												
Avg_Idle_Voff=	0.1	0.1	0.1	0.1	VDC	0.1	0.1	0.1	0	Pass	2.8	Pass
Error_Delay_Ted=	5343.8	5476.6	5640.6	5742.2	msec	5343.8	5742.2	5551	750	Pass	10000	Pass
Peak_Error_Delay_Ved=	2	2.1	2	2	VDC	2	2.1	2	0	Pass	20.5	Pass
Test Port Model Number:	3102	3102	3102	3102								
Test Port Hardware Version:	8	8	1	1								
Test Port Firmware Version:	3.2b	3.2b	3.26	3.26								