PSE Conformance Test Suite

July 2 2019 8:27 PM

Port Count..... 4
Loop Count..... 1
PSE Tested: **Sample Type-2 2-Event PSE**

Sifos Technologies

802.3at Conformance Report

version ***5.0.07***
report version 5.0.01

Test Mode: **30 Watt PHY**
Sifos Interop Index*: **86%**
Error Log: None

Chassis ID: 192.168.221.103
TestLoop: 1

	PSA-3000 Ports											
	1-1	1-2	2-1	2-2	UNITS	Min	Max	Average	Low Limit	P/F	High Limit	P/F
Test: det_v												
Open_Circuit_Det_Voc=	4.3	4.35	4.3	4.33	volts	4.3	4.35	4.32	2.8	Pass	30	Pass
Peak_Det_Vvalid=	9.31	9.3	9.28	9.28	volts	9.28	9.31	9.3	3.8	Pass	10	Pass
Min_Det_Vvalid=	3.99	4	3.99	4	volts	3.99	4	4	2.8	Pass	9	Pass
Det_Volt_Step_dVtest=	5.32	5.3	5.29	5.28	volts	5.28	5.32	5.3	1	Pass	7.2	Pass
Detection_Slew=	0.007	0.007	0.007	0.007	V/usec	0.007	0.007	0.007	0	Pass	0.1	Pass
Good_Sig_Det_Pulse=	1	1	1	1	edges	1	1	1	1	Pass	9	Pass
Backoff_Voltage=	0.1	0.1	0.1	0.1	volts	0.1	0.1	0.1	0	Pass	2.8	Pass
Non_802_Step_V=	0	0	0	0	volts	0	0	0	0	Pass	0.1	Pass
High_Sig_MaxV=	9.4	9.38	9.37	9.37	volts	9.37	9.4	9.4	3.8	Pass	11	Pass
Non_802_Discr_?=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Detect_Strategy=	1	1	1	1	****	1	1	1	0	Pass	2	Pass
Test: det_i												
Init_Current_Isc=	1.53	1.64	1.72	1.59	mA	1.53	1.72	1.62	0	Pass	5	Pass
Det_Current_Isc=	1.28	1.51	1.41	1.39	mA	1.28	1.51	1.4	0	Pass	5	Pass
Test: det_range												
Rgood_Max=	28	28	28	28	Kohm	28	28	28	26	Pass	32	Pass
Rgood_Min=	17	17	17	**15**	Kohm	15	17	16.5	16	**Fail**	19	Pass
Rmid_det=	28	28	28	28	Kohm	28	28	28	26	Pass	33	Pass
Cgood_Max=	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Rbad_Cbad_Stat=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Test: det_time												
Backoff_Time_Tdbo=	438	438	438	438	msec	438	438	438	-1	Pass	1500	Pass
Eff_Backoff_Tdbo_eff=	438	438	438	438	msec	438	438	438	-1	Pass	1500	Pass
Backoff_Type=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Detection_Time_Tdet=	287	287	287	287	msec	287	287	287	5	Pass	500	Pass
Total_Det_Time=	287	287	287	287	msec	287	287	287	5	Pass	1000	Pass
Test: det_rsource												
Regulated_Vstep_Zout=	0	0	0	0	KOhm	0	0	0	-0.1	Pass	12	Pass
Test: class_v												
Class_Voltage_Vclass=	17.3	17.2	17.1	17.1	volts	17.1	17.3	17.2	15.5	Pass	20.5	Pass
Vclass_Min=	17.1	17	16.9	16.8	volts	16.8	17.1	17	15.5	Pass	20.5	Pass
Mark_Voltage_Vmark=	9	8.9	8.9	8.9	volts	8.9	9	8.9	7	Pass	10	Pass
Mark_Voltage_Min=	8.9	8.9	8.9	8.9	volts	8.9	8.9	8.9	7	Pass	10	Pass
Test: class_time												
Event_Count=	2	2	2	2	****	2	2	2	2	Pass	3	Pass
Event1_Tcle1=	19.2	17.3	17.3	17.3	msec	17.3	19.2	17.8	5.6	Pass	30	Pass
Event2_Tcle2=	17.3	19.2	17.3	17.3	msec	17.3	19.2	17.8	5.6	Pass	30	Pass
Mark_Tme1=	7.7	7.7	7.7	9.6	msec	7.7	9.6	8.2	5.6	Pass	12.4	Pass
Mark_Tme2=	7.7	7.7	9.6	7.7	msec	7.7	9.6	8.2	5.6	Pass	376	Pass
Test: class_err												
Class_lim=	75	76	75	73	mA	73	76	75	51	Pass	100	Pass
Pwr_Cl_lim=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Pwr_Cl_55=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Mark_lim=	6	6	6	6	mA	6	6	6	5	Pass	100	Pass
Pwr_Cl_Uneven=	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Treset=	445	445	445	445	msec	445	445	445	15	Pass	10000	Pass
Test: pwrup_time												
Pwr-On_Rise_Time_Trise=	38	42	41	43	usec	38	43	41	15	Pass	50000	Pass
Power-On_Time_Tpon=	52.7	52.7	52.7	52.7	msec	52.7	52.7	52.7	0	Pass	400	Pass
Test: pwrup_inrush												
Init_Iinrush=	**861.63**	**867.25**	**861.5**	**863.88**	mA	861.5	867.25	863.6	400	Pass	450	**Fail**
Max_Iinrush_c4=	**501.75**	**502.75**	**501**	**501**	mA	501	502.75	501.6	400	Pass	450	**Fail**
Min_Iinrush=	**501.25**	**502.5**	**500.75**	**500.63**	mA	500.63	502.5	501.3	400	Pass	450	**Fail**
Tinrush=	**9999**	**9999**	**9999**	**9999**	msec	9999	9999	9999	50	Pass	75	**Fail**
Inrush_45m=	55.6	55.6	55.6	55.6	Volts	55.6	55.6	55.6	50	Pass	57	Pass
Inrush_Voltage=	54.7	54.8	54.8	54.8	Volts	54.7	54.8	54.8	30	Pass	57	Pass
Max_Init_Inrush=	944.5	929.3	929.3	929	mA	929	944.5	933	0	Pass	2000	Pass
Inrush_Strategy_c4=	3	3	3	3	****	3	3	3	0	Pass	1	Info
Test: pwron_v												
Vport_min_2=	54.7	53.9	54.8	54.8	V	53.9	54.8	54.6	50	Pass	57	Pass
Vport_max_2=	55.8	55.7	55.8	55.8	V	55.7	55.8	55.8	50	Pass	57	Pass
Vport_ripple_2=	4	4	4	5	mVpp	4	5	4.3	0	Pass	500	Pass
Vport_noise_2=	9	5	8	3	mVpp	3	9	6.3	0	Pass	200	Pass
Vtrans_min_2=	54.6	54.7	54.7	54.7	V	54.6	54.7	54.7	50	Pass	57	Pass
Vtrans_max_2=	55.7	55.8	55.8	55.8	V	55.7	55.8	55.8	50	Pass	57	Pass
Test: pwron_pwrcap												
Pcon_c4=	34.2	**28.3**	34.1	34.1	watts	28.3	34.2	32.7	28.7	**Fail**	38.9	Pass
Icon_%_c4=	117.8	**97.6**	117.4	117.5	%	97.6	117.8	112.6	100	**Fail**	9999	Pass
Type-2_Enable=	1	1	1	1	****	1	1	1	1	Pass	1	Pass
Test: pwron_maxi												
Ilim_Peak=	345	340.3	322.3	345	mA	322.3	345	338.2	0	Pass	1750	Pass
Ilim_Min_2=	686.1	687.8	684.9	684.8	mA	684.8	687.8	685.9	683	Pass	1750	Pass
Tlim_2=	62.5	62.9	62.9	62.1	msec	62.1	62.9	62.6	10	Pass	75	Pass
Vlim_2=	54.4	54.4	54.4	54.5	V	54.4	54.5	54.4	50	Pass	57	Pass
Ilim_Max_2=	861	867	861.5	863.5	mA	861	867	863.3	0	Pass	1750	Pass
Ilim_Low_V_Tol_2=	60.9	60.9	60.9	62.1	msec	60.9	62.1	61.2	10	Pass	9999	Pass
Ktran_lo_2=	108.9	108.9	108.9	109.1	%	108.9	109.1	109	92.4	Pass	115	Pass
Test: pwron_overld												
%Ipeak_2=	125	**96**	125	125	%	96	125	117.8	100	**Fail**	125	Pass
Vport_Ipeak_2=	54.5	53.9	54.6	54.6	V	53.9	54.6	54.4	50	Pass	57	Pass
Vport_5%DC_2=	54.5	53.8	54.6	54.6	V	53.8	54.6	54.4	50	Pass	57	Pass
Test: mps_dc_valid												
Min_Valid_Time_Tmps=	10	10	10	10	msec	10	10	10	1	Pass	60	Pass
Duty_Cycle_tol=	1	1	1	1	****	1	1	1	1	Pass	1	Pass
Test: mps_dc_pwrdn												
Min_Valid_I_hold=	8	8	8	9	mA	8	9	8.3	5	Pass	10	Pass
Time-to-Shutdown_Tmpdo=	355	355	355	355	msec	355	355	355	300	Pass	400	Pass
Max_Voltage_Vopen_max=	4.3	4.3	4.3	4.3	volts	4.3	4.3	4.3	-1	Pass	30	Pass
Test: pwrdn_overld												
Icut_2=	630	536	630	640.5	mA	536	640.5	609.1	-1	Pass	1750	Pass
Tcut_2=	58.6	66.4	58.6	58.6	msec	58.6	66.4	60.6	10	Pass	9999	Pass
Isoft_2=	-1	-1	-1	-1	mA	-1	-1	-1	-1	Pass	683	Pass
Tsoft_2=	-1	-1	-1	-1	msec	-1	-1	-1	-1	Pass	2000	Pass
Test: pwrdn_time												
Turn-Off_Time_Toff=	50.7	61.7	40.2	10.5	mSec	10.5	61.7	40.8	0	Pass	500	Pass
Output_Cap_Cout=	0.1069	0.098	0.1138	0.1218	uF	0.098	0.1218	0.11	-1	Pass	0.52	Pass
Output_Load_Rp=	338	687	198.7	**32.8**	Kohm	32.8	687	314	45	Info	50000	Pass
Test: pwrdn_v												
Avg_Idle_Voff=	0.1	0.1	0.1	0.1	VDC	0.1	0.1	0.1	0	Pass	2.8	Pass
Error_Delay_Ted=	1281.3	1281.3	1273.4	1281.3	msec	1273.4	1281.3	1279	750	Pass	10000	Pass
Peak_Error_Delay_Ved=	0.6	0.6	0.5	0.6	VDC	0.5	0.6	0.6	0	Pass	20.5	Pass
Test Port Model Number:	**3202**	**3202**	**3202**	**3202**								
Test Port Hardware Version:	8	8	8	8								
Test Port Firmware Version:	**4.13**	**4.13**	**4.13**	**4.13**								