PSE Conformance Test Suite 5.x.x (PSA-3000) Tests and Parameters

Parameter	Description	Additional Information	802.3at		802.3bt	
			Clause	PICS	Clause	PICS
Test: det_v						
Open_Circuit_Det_Voc=	Peak Open Circuit Detection Voltage		33.2.4.1	PSE5	145.2.5.1	PSE6
Peak_Det_Vvalid=	Maximum Detection Voltage with Valid Detection Signature		33.2.5.1	PSE11	145.2.6.1	PSE10
Min_Det_Vvalid=	Minimum Valid Step Voltage with Valid Detection Signature		33.2.5.2	PSE13	145.2.6.2	PSE12
Det_Volt_Step_dVtest=	Minumum 802.3at Voltage Step Magnitude	*If dVtest step size measures under 1 Volt, then it may be that the PSE is using alternate steps to make the resistance measurement. If "Info" appears with this parameter, then Good_Sig_Det_Pulse must be 2 or more steps, or this is a "FAIL".*	33.2.5.2	PSE16 PSE17 PSE18	 145.2.7 145.2.10.11	PSE15 PSE16 PSE17 PSE21 PSD75
Detection_Slew=	Maximum Step Slew Rate					
Good_Sig_Det_Pulse=	Number of Valid Detection Transitions (i.e. between valid step levels)					
Backoff_Voltage=	IDLE State voltage during detection backoff					
Non_802_Step_V=	Peak Non-802.3at (< 2.8 Volt) Step Voltage Level	*Test is exposing that PSE may be using additional signaling and measurements prior to or as part of normal 802.3at detection measurements. These may be beneficial in limiting detection pulse power to a non-PD device, however they are not part of the standard.*				
High_Sig_MaxV=	Maximum Detection Voltage with High Detection Signature	*The 802.3at specification does not define requirements for detection signaling when detection load is slightly outside valid range.*				
Non_802_Discr_?=	This binary indicator is set to "1" when a PSE is determined to be using means other than normal 802.3at detection measurements to resolve the valid detection range.	*While not required by the standard, one would expect to see normal 802.3at detection pulses when PD signatures are somewhat out of the valid band. Some PSE's withold 802.3at detection measurements until the signature is virtually inside the valid detection band.*				
Detect_Strategy=	Type 0: Normal 802.3at Detection Methods Type 1: Proprietary Pre-Detection Observed with Open Circuit Type 2: Zero-Backoff Type PSE Port Determined Type 3: Open Circuit Signaling Includes 50V Legacy Detection Pulses Type 4: Proprietary Pre-Detection Observed with Open Circuit - Open Circuit Voltage outside PD Detection Voltage Band Type 5: Zero-Backoff Type PSE Determined - Open Circuit Voltage outside PD Detection Voltage Band	*This parameter categorizes PSE port detection strategy into one of 6 categories. Pre-Detection Only indicates PSE does not form full 802.3at detection pulses until a near valid detection signature is present. Zero-Backoff means the PSE does not have distinct backoffs during open circuit detection. 50V Pulses refers to existance of legacy detection pulses prior to any PD connection. Type 4 and 5 indicate that the open circuit detection signaling is entirely above the required PD signature band and thus PSE is relying on PD Detection Signature to be visible outside the minimum specified valid signature band.*				
Test: det_i						
Init_Current_Isc=	Peak Current Flow During Detection Below 2.8 Volts		33.2.5.1	PSE13	145.2.6.2	PSE12
Det_Current_Isc=	Peak Current Flow During Detection Above 2.8 Volts					
Test: det_range						
Rgood_Max=	Maximum Valid Detection Signature Resistance		33.2.5	PSE9	145.2.6	PSE9
Rgood_Min=	Minimum Valid Detection Signature Resistance		33.2.5.3	PSE10	145.2.6.3	PSE18
Rmid_det=	Maximum (or Minimum) Detection Signature producing a power-up given connections with various time alignments to the detection measurement.	*Assess if detection measurement is sensitive to when the detection signature is connected.*		PSE19 PSE20	145.2.6.4	PSE19
Cgood_Max=	Maximum Valid Detection Signature Capacitance					
Rbad_Cbad_Stat=	PSE response to marginally invalid Rdet + lowest rejected Cdet value	*Determine if adding capacitance causes a high detection signature to become valid to PSE.*				
Test: det_time						
Backoff_Time_Tdbo=	Backoff Time Between Detection Pulses	*With ALT B PSE's, strict requirement is minimum 2 seconds. With ALT A PSE's, IEEE recommended requirement is that a second detection cycle complete within 2 seconds of the first detection cycle completing, however this is not a strict requirement. Report will "Info" ALT A PSE's with longer than 1.5 second backoff, allowing 500msec for detection time.*	33.2.7	PSE47	145.2.5 145.2.5.1 145.2.10	PSE4 PSE5 PSE57
Eff_Backoff_Tdbo_eff=	Effective Backoff Time Following Invalid Signature Measurement - measures time from invalid detection until valid detection producing a power-up.					
Backoff_Type=	Type 0: Normal 802.3at Detection Backoffs Type 1: Non-802.3 Signaling Detected Type 2: 50 Volt Legacy Detection Pulses Detected Type 3: PoH Double-Detection Scheme	*For the most part, none of these are problems. The 50V Legacy Detection pulse will place 50V common mode on the PD connection if an invalid PD signature is measured on the first attempt by the PSE port. Non-802.3 signaling usually indicates proprietary detection assessments. PoH Double Detection causes detection back-off to become ambiguous.*				
Detection_Time_Tdet=	Duration of 802.3at Detection Measurements	*Measured only over 802.3at Min to Max detection levels.*				
Total_Det_Time=	Total Duration of Detection Pulse	*Measured over exactly one cycle of detection.*				
Test: det_rsource						
Output_Impedance_Zout=	PSE Effective Output Impedance During PD Detection given a current-sourcing detection scheme	*det_rsource cannot determine if PSE output is diode protected or if reverse input resistance = Zout. Rp (pwrdn_time) MAY be a more accurate indication of Rrev. Maximum value reported will be 450K Ω as this is highest Zout that can be resolved by the measurement technique.*	33.2.5.1	PSE12	145.2.6.1	PSE11
Regulated_Vstep_Zout=	PSE Effective Output Impedance During PD Detection given a regulated voltage detection scheme (e.g. LOW or Zero effective Zout)					
Test: class_v						
Class_Voltage_Vclass=	Average Classification Step Voltage Level	*Pertains to all PSE's that do PHY classification*	33.2.6.1	PSE25	145.2.8	PSE38
Vclass_Min=	Minimum Class Voltage given Maximum Valid Class Signature		33.2.6.2	PSE26	145.2.8.1	PSE40
Mark_Voltage_Vmark=	Average Mark Region Voltage Level for 2-Event, Type 2 PSE's only	*Mark Region is only tested when High Power Grant Type is PHY and Type-2 (or 30W) Power Mode is tested. The PSA-3000 simulates true Mark Loads while the PSA-1200 does not meaning test limits are only enforceable with the PSA-3000.*		PSE33 PSE36 PSE44 PSE45		PSE42 PSE44 PSE49 PSE50 PSE52 PSE53
Mark_Voltage_Min=	Minimum Mark Region Voltage with Maximum Valid Mark Load Current					
Class_Reset_V=	For Type-3 BT 2-pair PSEs. Maximum value of the Class Reset Voltage after a Class Probe and prior to Classification					
Test: class_time						
Class_Time_Tpdc=	Classification Time Duration		33.2.4.4	PSE6	145.2.8	PSE27
Event_Count=	Classification Pulse (Or Event) Count	*Must be 1 or 0 Events for Type 1 PSE's, must be at least 1 Event for Type 2 PSE's. May be 2 Event for Type-2 PSE's that use 2-Event Power Grants. Note: 3 Events (3 class pulses) will be accepted because while it violates the PSE State diagram, it is compliant to the PD State Diagram meaning PD's must anticipate the possibility of a third classification step.*	33.2.4.6 33.2.6 33.2.6.1 33.2.6.2	PSE7 PSE21 PSE27 PSE29 PSE34 PSE37 PSE38 PSE39 PSE43	145.2.8.1	PSE29 PSE30 PSE32 PSA36 PSE38 PSE40 PSE41 PSE43 PSE45 PSE50 PSE51 PSE52
Event1_Tcle1=	Duration of first Class Event (or Pulse) for Type 2, 2-Event PSE	*Reported with 802.3at PSE's.*				
Event1_Tlce=	Duration of the LCE Event for Type 3 PSEs	*Reported with 802.3bt Type-3 PSE's*				
Event2_Tcle2=	Duration of second Class Event (or Pulse) for Type 2, 2-Event PSE					
Mark_Tme1=	Duration of first Mark Event (or Pulse) for Type 2, 2-Event PSE	*This measurement is not tested to a PASS/FAIL limit because the present PSA Test Blade will not furnish the required Mark Region current to discharge the PSE port following each PSE classification measurement.*				
Mark_Tme2=	Duration of second Mark Event (or Pulse) for Type 2, 2-Event PSE					
Class_Probe_Events=	For Type-3 BT 2-Pair PSEs. Number of Class Events in the Class Probe	*Reported with 802.3bt Type-3 PSE's*				
Class_Reset_Time=	For Type-3 BT 2-Pair PSEs. Time duration of a Class Reset after a Class Probe and Prior to Classification					
Test: class_err						
Class_lim=	Maximum Class Current PSE will support before current limiting		33.2.6	PSE23	145.2.5	PSE4
Pwr_Cl_lim=	PSE Power-Up Response to Current-Limited Class Current	*Type-2 PSE's should not apply power*	33.2.6.1	PSE24	145.2.8.1	PSE30
Pwr_Cl_55=	PSE Power-Up Response to 55mA (non-valid) Class Signature	*Type-2 PSE's should not apply power*	33.2.6.2	PSE31		PSE46
Mark_Lim=	Maximum Mark Current supported during a 2-event Mark Region			PSE32		PSE47
Pwr_Cl_Uneven=	PSE Power-Up Response to Unequal Class Currents in 2 Event Signature	*Type-2 PSE's should not apply power*		PSE40		PSE48
Treset=	Duration of IDLE Region following Unequal Class Current Signature	*PSE should IDLE for at least 15 msec*		PSE41 PSE42 PSE46		
Test: class_lldp						
PSE_Source_Priority=	Binary indication of Valid (=0) or Invalid (=1) PoE+ Source/Priority Field	*Should report "PSE", Type 1 or Type 2, "0" in Reserved Fields*	33.2.4.4	PSE6	145.5.1	DLL1
PSE_MDI_Pwr_Sup=	Binary indication of Valid (=0) or Invalid (=1) MDI Capabilities Field	*Proper values are 0x07 or 0x0F according to Clause 79*	33.2.4.6	PSE7	145.5.2	DLL2
PSE_LLDP_Time_n=	Time from Power-Up until Receipt of First PoE LLDP Packet from PSE given Type "n" (1 or 2) mode PD Emulation	*Type 2 PSE's must provide packet within 10 seconds of entering the Power-On state*	33.2.6	PSE21	145.5.3	DLL8
PSE_LLDP_Type_n=	PSE Type Communicated in PoE+ Source/Priority Field given Type "n" (1 or 2) mode PD Emulation.	*Must be 1 or 2*	33.6 33.6.1	DLL1 DLL2	79.3.2 79.3.2.5	DLL9 PVT3
PSE_Echo_Time_n=	Time for PSE to Echo PD Power Request given Type "n" (1 or 2) mode PD Emulation.	*Requirement is in 10 seconds or less*	33.6.2 33.6.3	DLL3 DLL4	79.3.2.6	PVT18 PVT19
PSE_Alloc_Pwr_n=	Power Allocated to PD at Startup given Type "n" (1 or 2) mode PD Emulation.	*Should be >= to PD Request (8.1 W for Type-1, 20.3W for Type-2)*		DLL5 DLL9		
PSE_Alloc_Time_n=	Time for PSE to Allocate PD Power Request given Type "n" (1 or 2) mode PD Emulation.	*Soft limit of 30 seconds used - this is not strictly specified in 802.3at.*				
PD_Power_Adjust_n=	Power Allocated to PD following a Power Adjustment Request to Maximum Power Allowed given Type "n" (1 or 2) mode PD Emulation.	*Should be = to PD Request (13 W for Type-1, 25.5W for Type-2)*				
PSE_Adjust_Time_n=	Time for PSE to Echo PD Power (Adjustment) Request given Type "n" (1 or 2) mode PD Emulation.	*Requirement is in 10 seconds or less*				

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Parameter	Description	Additional Information	802.3at		802.3bt	
Link_Down_Shutdown_?=	Indicator of PSE response when LAN link drops after powering and negotiating with a PD. 0= POWERED, 1= POWER_REMOVED.	*Test evaluates power status 12 seconds after LAN Link Drop. PSE's that drop power are at risk interoperating with PD's that deliberately shut down PHY's.*				
PSE_Alloc_Pwr_bt_tlv_n=	For Type-3 BT 2-pair PSEs. 2 > at_tlv value, 1 = at_tlv value, 0 < at_tlv value. -1 if PSE did not transmit BT TLVs	*If PD Emulation is done using a PSA-3102 test blade, then BT TLVs are not supported. This will result in a -1 result that will FAIL. PSA-3202 test blades should be used for Testing Type-3 PSE's that utilize LLDP.*				
PD_Power_Adjust_bt_tlv_n=	For Type-3 BT 2-pair PSEs. 2 > at_tlv value, 1 = at_tlv value, 0 < at_tlv value. -1 if PSE did not transmit BT TLVs					
Test: pwrup_time						
Pwr-On_Rise_Time_Trise=	Rise Time of Power-Up Edge	*Fastest rise time that can be measured is 6usec. If -99, then rise time measurement likely false triggered on a large voltage transient most likely at start or end of classification pulse.* *As of report version **5.1.04**, this parameter is PASS/**INFO** and not PASS/**FAIL** because technically speaking, the explicit measurement of 10% to 90% of **Vpse** is not possible with the PSA time interval measurement and would not be feasible using any method if the PSE powers up from Vmark (2-Event classification). A rise time measurement with an **INFO** mark indicates a power-up slew rate that exceeds the 'intent' of the 802.3 standard.*	33.2.7	PSE47	145.2.5 145.2.10 145.2.10.14	PSE4 PSE57 PSE80
Power-On_Time_Tpon=	Time Duration from End of Detection Until Power-Up	*Measured from the final complete detection prior to the power-up event.*				
Test: pwrup_inrush						
Init_Iinrush=	Peak Inrush Current between 1 and 3 msec of current-limiting inrush overload.		33.2.7 33.2.7.5	PSE47 PSE54 PSE55	145.2.5 145.2.10.7	PSE4 PSE57 PSE68 PSE69
Max_Iinrush_cN=	Maximum In-Rush Load Current Supplied During After 1 msec given Class N power-up.	*Upper limit is 450 mA. Lower limit of 0 since this parameter is only compared to an upper limit.*				
Min_Iinrush=	Minimum In-Rush Load Current Supported During First 45 msec.	*Inrush Current must be above 400mA if Vport ≥30V and above 60 mA if Inrush Voltage is measured between 10 and 30 volts. PSA active load in saturation is 62 ohm, so Vport will likely be between 20 and 30 VDC.*				
Inrush_Voltage=	Average Output Voltage from 5 to 45 msec During 400 mA In-Rush Load. In the event of power foldback, Vinrush is measured over a 5 msec period coincident with 65mA load immediately following the current limiting overload removal. Minimum voltage allowed is 10V.	*A PSE must support 400 mA of inrush current during power-up so long as port voltage (Inrush_Voltage) remains above 30VDC.*				
Tinrush=	Time from onset of inrush current-limiting overload until port shut-down by the PSE.	*Tinrush is capped at 100msec, the duration of the inrush load transient applied.*				
Inrush_45m=	Power-Up Response to a current-limiting Inrush overload of duration 45 msec, or less than Tinrush (MIN).	*Inrush overloads less than duration Tinrush(MIN), or 50 msec, should not prohibit port power-ups.*				
Max_Init_Inrush=	Peak In-Rush Load Current Allowed During First 1 msec	*Testing examines various inrush overloads up to 1000 mA*				
Inrush_Strategy_cN=	Determines if Port Voltage or **Tinrush** Time is used to mark the end of the Power Up (Inrush) processing state. If Voltage is used, characterizes subsequent current limiting behavior given Class N power-up. 0 = Time (802.3at recommended) 1= Voltage, current limited @ **Ilim_1** (< 450mA) for **Tlim_1** (50-75 msec) 2= Voltage, current limited @ **Ilim_1** (< 450mA) for > **Tlim_1(max)** 3= Voltage, current not limited @ **Ilim_1** (< 450mA) and/or no inrush shutdown 4= Voltage, current limited @ **Ilim_1** (< 450mA) + low voltage shutdown	*A PSE using the voltage method (legacy_powerup exception in 802.3at) will not necessarily limit inrush current to a PD that delays its inrush load by even just one millisecond. This could damage a PD that is expecting inrush PSE-based limiting. If **Inrush_Strategy_cN** is 1, the PSE is using Type-1 **Ilim** and **Tlim** to produce a shutdown after 50 msec and before 75 msec while limiting to 450mA or less, so this is almost as good as the recommended **Tinrush** processing. Values 2 and 3 produce INFO warnings as they risk damage to a PD. Value 4 produces INFO warning as it may prohibit PD powering. With Type-3 (802.3bt) PSE's, **Inrush_Strategy** must report 0 or test will FAIL.*				
Test: pwron_v						
Vport_min_n=	Minimum DC Port Voltage measured with minimum and maximum Port Loading for Type "n" PD emulation		33.2.4.6 33.2.7 33.2.7.1 33.2.7.3	PSE8 PSE47 PSE48 PSE52	145.2.10 145.2.10.1 145.2.10.3 145.2.10.5	PSE57 PSE58 PSE61 PSE64
Vport_max_n=	Maximum DC Port Voltage measured with minimum and maximum Port Loading for Type "n" PD emulation					
Vport_ripple_n=	Maximum AC Ripple (20Hz - 500Hz) Vpp measured with minimum and maximum Port Loading for Type "n" PD emulation	*Goal is to detect line voltage ripple and AC MPS signaling components below 400 Hz. NOTE: A "-1" reading indicates a possible hardware failure and should be reported to Sifos Technologies.*				
Vport_noise_n=	Maximum AC Noise (10KHz - 350KHz) Vpp measured with minimum and maximum Port Loading for Type "n" PD emulation	*Goal is to assess noise from DC-DC power conversion components in the 2KHz - 400KHz band. NOTE: A "-1" reading indicates a possible hardware failure and should be reported to Sifos Technologies.*				
Vtrans_min_n=	Minimum Port Voltage measured during a rapid (< 5 msec) load excursion between ~ .5W to Pclass and back	*Sampled at ~ 40 usec periodicity. When testing Type-2 PSE's, transient voltage samples following a 250 usec "Ktran_lo" duration are evaluated for Vport_min (50V) criteria.*				
Vtrans_max_n=	Maximum Port Voltage measured during a rapid (< 5 msec) load excursion between ~ .5W to Pclass and back					
Test: pwron_pwrcap						
Pcon_c0=	PSE Power Capacity to a Class 0 PD	*Type-1 PSE's are tested with PD Class 0-3 emulations to assess if power is restricted to allowable levels give PD classification (i.e. power "policing"). Type-2 PSE's should be tested in the 15.4W mode to assess these behaviors. The power output, Pclass, required from a PSE port is calculated as as function of PSE port voltage at full load capacity using IEEE 802.3at equation 33-3. The load current at full capacity is then ratio'd to Pclass / Vport_pse to produce Icon_%.*	33.2.4.6 33.2.6 33.2.6.1 33.2.6.2 33.2.7 3.2.8	PSE8 PSE22 PSE28 PSE29 PSE30 PSE35 PSE43 PSE47 PSE63	145.2.8 145.2.10.6 145.2.10.7 145.2.11	PSE29 PSE65 PSE68 PSE82
Icon_%_c0=	Load Current Capacity Ratio to Icon = Pclass / Vport_pse to Class 0 PD					
Pcon_c1=	PSE Power Capacity to a Class 1 PD					
Icon_%_c1=	Load Current Capacity Ratio to Icon = Pclass / Vport_pse to Class 1 PD					
Pcon_c2=	PSE Power Capacity to a Class 2 PD					
Icon_%_c2=	Load Current Capacity Ratio to Icon = Pclass / Vport_pse to Class 2 PD					
Pcon_c3=	PSE Power Capacity to a Class 3 PD					
Icon_%_c3=	Load Current Capacity Ratio to Icon = Pclass / Vport_pse to Class 3 PD					
Pcon_c4=	PSE Power Capacity to a Class 4 PD	*Test will return only Class 4 power capacity when run with 30W (Type-2) power mode.*				
Icon_%_c4=	Load Current Capacity Ratio to Icon = Pclass / Vport_pse to Class 4 PD					
Type-2_Enable=	Verify that Class 4 Power is available 80 msec following a PHY (or 2-Event) power grant. 1= "AVAILABLE", 0= "NOT AVAILABLE"	*Only tested given 30W PSE's. PSE must make 30W available within 80 msec of power-up if 30W Grant is "PHY" and should not allow 30W power within 80msec if 30W Grant is "LLDP".*				
Pclass_LLDP_22.7=	Indicator as to whether the PSE supported a Pclass_pse power level following a 22.7 watt LLDP power allocation. 0= FAIL, 1= PASS.	*Purpose is to search for flaws in LLDP power allocation algorithms. Value will be -1 for non-LLDP granting PSE's, when testing with Type-1 PD emulation, and if PSE fails to allocate requested power.*				
Pclass_LLDP_24.5=	Indicator as to whether the PSE supported a Pclass_pse power level following a 24.5 watt LLDP power allocation. 0= FAIL, 1= PASS.					
Test: pwron_maxi						
Ilim_Peak=	Maximum output current over 8-75msec from PSE given a 1.95A load pulse with foldback suppression applied. PSE must limit to < 1.75A.	***Ilim_min** is completely redefined in 802.3at and 802.3bt to represent a MINIMUM transient current level that a PSE port must support for a minimum duration of **Tlim_Min**. For Type-1 and 15W Type-3 PSE's (Type-1 PD emulation), the PSE must support 400mA for 50 msec. For Type-2 and 30W Type-3 PSE's, the PSE must support 684 mA for 10 msec assuming port voltage does not drop below **Vpse_min**. Given these loads, the PSE should support a port voltage of **Vpse_min** or higher.* ***Tlim_max** with Type-3 PSE's is tested using an 850mA load rather than **Ilim_min** in accordance with the Type-3 current template in clause 145.*	33.2.7 33.2.7.2 33.2.7.7	PSE47 PSE50 PSE56 PSE57 PSE58	145.2.10.3 145.2.10.9	PSE57 PSE61 PSE71 PSE72 PSE73
Ilim_Min_n=	Minimum load current available given 50msec, (Ilim_Min+2mA) load pulse with foldback suppression applied given Type "n" PD.					
Tlim_n= or Tlim_min_n=	Time until power removal given an Ilim_Min load pulse (no foldback suppression). **Tlim_min_n** reported with TYPE-3 PSE's.					
Tlim_max_n=	TYPE-3 PSE Only: Time until power removal given an 850mA load pulse with foldback suppression.					
Vlim_n=	Port Voltage measured during Ilim_Min load pulse (no foldback suppression)					
Ilim_Max_n=	Peak output current from 1 to 75 msec given a > Ilim_Min (700mA - 1000mA) load pulse using foldback suppression.	*Informational only, no limits.*				
Ilim_Low_V_Tol_n=	Time until power removal given a 100msec load pulse including max transition band current (no foldback suppression). Load pulse magnitude is 460mA for Type-1 and 1000mA for Type-2 mode testing.	*Informational only, no limits. Evaluating to see if PSE removes power immediately with low voltage condition that accompanies current limiting.*				
Ktran_lo=	Excursion below 50V given a 250usec, 686mA load pulse when testing Type-2 PSE's. In 802.3bt (clause 145), this parameter is named **Vtrans_2p**.	*Type-2 PSE should regulate voltage to stay above 92.4% of Vpse_min, or 46.2V given described transient.*				
Test: pwron_autoclass						
Autoclass_Shutdown=	Set PSE power to 95% of Pclass and determine if PSE removes power	*This is an INFO only paramter. If PSE removes power set to 1 otherwise set to 0. A value of 0 implies that the PSE does not support Autoclass. The remaining parameters will not be tested and values will be set to 99.*			145.2.8.1 145.2.8.2	PSE24a PSE39 PSE54 PSE55
Pac_margin_C3_low=	PSE powers 3W in Class 3 and determines that PSE maintains power at Pautoclass + Pac_margin. Pac_margin for Class 1-4 is 0.5 W.	*If PSE remains powered set to 1 otherwise set to 0. If PSE determined to not support Autoclass then set to 99.*				
Pac_margin_C3_high=	PSE powers 9W in Class 3 and determines that PSE maintains power at Pautoclass + Pac_margin. Pac_margin for Class 1-4 is 0.5 W.					
Pac_margin_C4_low=	PSE powers 3W in Class 4 and determines that PSE maintains power at Pautoclass + Pac_margin. Pac_margin for Class 1-4 is 0.5 W.					
Pac_margin_C4_high=	PSE powers 16W in Class 4 and determines that PSE maintains power at Pautoclass + Pac_margin. Pac_margin for Class 1-4 is 0.5 W.					
Autoclass_4W=	Powers PSE with Pautoclass < 4W then applys 95% of Pclass. Verifies that PSE remains powered.	*Parameter from Supplemental Spec 802.3cv. Returns 1 if PSE remains powered otherwise set to 0. If PSE does not support Autoclass then value is set to 99.*				
Test: pwron_overld						

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Parameter	Description	Additional Information	802.3at		802.3bt	
%Ipeak_n=	The % relative to Ipeak current that the PSE will support in a load transient of at least 50msec duration (Tovld_min) given Type-"n" PD emulation.	*Must support at least 100% of Ipeak for 50 msec.* ***Ipeak*** *computed from formula 33-4.*	33.2.6 33.2.7.2 33.2.7.4	PSE22 PSE51 PSE53	145.2.10.3 145.2.10.6 145.2.11	PSE57 PSE62 PSE66
Vport_Ipeak_n=	Minimum port voltage measured during the I= Ipeak transient load pulse given	*Port voltage must be* ***≥ Vpse_min***	33.2.8	PSE63		PSE82
Vport_5%DC_n=	Minimum port voltage measured with 50msec Ipeak transient loads applied once per second over a 10 second interval given Type-"n" PD emulation.					
Test: mps_dc_valid						
Min_Valid_Time_Tmps=	Maximum time over which a PSE can decide to reset it's **Tmpdo** timer given a VALID DC MPS load level. 802.3at (clause 33) PSE's should reset Tmpdo timer with 60msec or less of valid MPS current. 802.3bt (clause 145) PSE's should reset Tmpdo timer with 6msec or less of valid MPS current.	*The description in the 802.3at standard is vague and requires careful inspection to intepret properly. Tmps is presented as a "MINIMUM" limit which makes sense from the PD point of view but is not as clear from the PSE point of view. Use "Show Traces" to witness the minimum required "on" time.*	33.2.7 33.2.9.1.2	PSE47 PSE68 PSE71	145.2.10 145.2.12	PSE57 PSE83 PSE84 PSE85 PSE87
Duty_Cycle_tol=	Assesses PSE maintain power status (Vport) with a multi-cycling DC MPS valid/non-valid load with 20% "on" duty-cycle using 25mA valid load and Tmps_Min "on" times.	*PSE should maintain power continuously - 5 off/on cycles sequenced. Use "Show Traces" to witness the duty cycle.*				
Test: mps_dc_pwrdn						
Min_Valid_I_hold=	Low Current Threshold Required to Force PSE Shut-Down	*802.3at (clause 33) and 802.3bt (clause 145) have different requirements for I_hold. Valid values are 5-10 mA for 802.3at and 4-9 mA for 802.3bt PSE's.*	33.2.7 33.2.9.1.2	PSE47 PSE69 PSE70	145.2.10 145.2.12	PSE57 PSE83 PSE85
Time-to-Shutdown_Tmpdo=	Time Duration from PD Disconnect Until Power-Down Initiated (DC MPS)	*802.3at (clause 33) and 802.3bt (clause 145) have different requirements for Tmpdo. Valid values are 300 msec-400msec for 802.3at and 320-400msec for 802.3bt PSE's.*				PSE86
Max_Voltage_Vopen_max=	Max port signaling voltage following disconnect power-down	*This parameter is not specified explicitly for DC MPS as it is for AC MPS, however implicitly, this voltage should not exceed Voc.*				
Test: pwrdn_overld						
Icut_n=	Minumum sub-**Ilim(n)** load current causing power-down for Type-"n" PD Emulation given a 75 msec transient pulse and Type-"n" PD emulation.	*Qualifying shutdowns must occur during or shortly after 75msec transient duration. Under-powered PSE's will report a NEGATIVE* ***Icut_n*** *value. Report '-1' if* ***Icut_n*** *not found below* ***Ilim_Min*** *for Type* ***n****.*				
Tcut_n=	Time from start of **Icut_n** load transient until port shutdown - will be capped at duration of the **Icut_n** load transient even if the shutdown occurs up to 2 seconds following the start of transient.	*Given an* ***Icut*** *shutdown,* ***Tcut*** *will always fall between 0 and 75 msec. Reports 9999 no* ***Icut*** *shutdown produced. Allows for PSE's that measure elapsed time* ***Tcut*** *over a longer time window.*				
Isoft_n=	Minumum load current up to or marginally exceeding **Ilim_min** that causes a shutdown for Type-"n" PD Emulation given a 2 second transient pulse and Type-"n" PD emulation.	*This measurement determines if PSE is likely invoking a firmware managed overload shutdown decision process. Underpowered PSE's will report a NEGATIVE* ***Isoft_n*** *value.* ***Tsoft_n*** *can range up to 4 seconds. Reports -1 for* ***Isoft*** *and* ***Tsoft*** *if* ***Isoft*** *is not found.*				
Tsoft_n=	Time from start of **Isoft_n** load transient until port shutdown - will be capped at duration of the **Isoft_n** load transient even if the shutdown occurs up to 2 seconds following the start of transient.					
Test: pwrdn_time						
Turn-Off_Time_Toff=	Turn-Off Time (Assuming Effective 320 Kohm PD Load)		33.2.5.1	PSE12	145.2.6.1	PSE14
Output_Cap_Cout=	Effective PSE Port Output Capacitance During Power-Down	*Cout measurement is accurate to approximately .1 uF.*	33.2.7.8	PSE15	145.2.10.10	PSE57
Output_Load_Rp=	Effective PSE Shunt Port Resistance During Power-Down. This will generally be the same as Rrev in the 802.3at specification.	*Rp approximates PSE resistive discharge load during PSE port power-down. It is very possible, but not certain, that this could equate to Rrev which is specified to be > 45Kohm. The measurement is accurate to approximately 3 Kohms.*		PSE59		PSE74
Test: pwrdn_v						
Avg_Idle_Voff=	Average IDLE State Voltage Following Power-Down		33.2.7.9	PSE60	145.2.5	PSE4
Error_Delay_Ted=	Time from an overload shutdown until the next power-up is enabled.	*802.3af Maintenance Request 1117 redfined error delay processing to allow detection and classification during the error delay interval so long as power-up is inhibited. The 802.3at and 802.3bt PSE state machines include this optional PSE behavior.*			145.2.10	PSE57
Peak_Error_Delay_Ved=	Peak PSE Port Voltage during Error Delay time interval preceding final detection leading to the next power-up. Acts as indicator of a PSE that does detection and classification during Ted.				145.2.10.11	PSE75 PSE76
Test: mps_ac_pwrdn						
Power_Down_Time_Tmpdo=	Time Duration from PD Disconnect Until Power-Down Initiated (AC MPS)		33.2.9.1.1	PSE65		
DC_Max_Load_Imin1=	DC Load Current Required To Enable AC MPS Power-Down	*Must be 0 mA in 4.x.x Test Suite, up to 10mA allowed in 3.x.x Test Suite*		PSE66 PSE67		
Test: mps_ac_vf						
AC_MPS_V_open=	Pk-Pk AC Voltage Following PD Disconnect		33.2.9.1.1	PSE64		
AC_MPS_V_open%=	Pk-Pk AC Voltage reported as a % of Vport					
AC_MPS_Frequency=	AC MPS Signal Frequency					
Slew_Rate=	Peak AC MPS Signal Slew Rate					
Source_Current_Isac=	Approximate Current Compliance (Limit) Associated with AC MPS Signal					
Test: mps_ac_voff						
Peak_AC_MPS_V_open1=	Peak Port Voltage Measured Following PSE Shut-Down					
Peak_Disconnect_Vport=	Peak Absolute Voltage Measured Following PD Disconnect					

802.3at PICS Not Tested	802.3bt PICS Not Tested
PSE14: No capability to drive current into PSE port - this would risk damage to PSE port	PSE13: See 802.3at PSE14
PSE49: No ability to adjust current at 35mA/usec and no assurance that a measurable slew rate would occur	PSE59: See 802.3at PSE49
PSE61: No ability to measure individual conductor currents nor to create ideal external balance	PSE70: No ability to measure inrush current with PSE voltage between 5 and 30V
PSE62: No abilit to measure LAN Differential pulse characteristics (droop)	PSE77: See 802.3at PSE61
	PSE78: See 802.3at PSE62

802.3at PICS Tested Implicitly or Reduntantly	802.3bt PICS Tested Implicitly or Only Relevant to 4-Pair PSE's
PSE1: Test Suite tests Endspans and Midspans	PSE1: Type-4 Polarity Configuration with Limit Check in Test Report Header
PSE2: Test won't operate unless Alt-A or Alt-B implemented	PSE2: Test won't operate unless PSE is valid Alt-A or Alt-B
PSE3: Tests are organized by State Machine functions	PSE3: Test won't operate unless PSE is valid Alt-A or Alt-B
PSE4: Redundant with other PICS (e.g. PSE27, PSE29, PSE47)	PSE7: Applies to 4-Pair PSE's performing detection/connection check
	PSE8: This is primarily applicable to 4-Pair PSE's
	PSE20: Applies to 4-Pair PSE's that do connection check
	PSE21: Applies to 4-Pair PSE's that do connection check
	PSE22: Applies to 4-Pair PSE's that do connection check
	PSE23: Applies to 4-Pair PSE's that do connection check
	PSE24: Applies to pairset power removal from 4-Pair powering
	PSE25: Applies to pairset power removal from 4-Pair powering
	PSE26: Applies to pairset power removal from 4-Pair powering
	PSE28: Applies to Dual Signature PD detection
	PSE31: Applies to Dual Signature PD classification
	PSE33: Applies to Dual Signature PD classification
	PSE34: Applies to Type-4 PSE's
	PSE35: Applies to Type-4 PSE's
	PSE37: Applies to Dual Signature PD classification
	PSE53: Applies to Dual Signature PD classification
	PSE56: Pertains to 4-Pair ID
	PSE60: Applies to 4-Pair Powering
	PSE63: Applies to 4-Pair Powering
	PSE67: Applies to 4-Pair Powering
	PSE76: Applies to Dual Signature PD powering
	PSE79: Applies to 4-Pair Type-4 PSE powering
	PSE81: Applies to Dual Signature PD powering
	PSE88 - PSE96: All apply to 4-Pair Powering

802.3at Summary		802.3bt Summary	
Total PSE / Applicable DLL PICS	80	Total PSE / Applicable DLL PICS	100
Total Tested	76	Total Tested	95
% Covered	95%	% Covered	95%