4-Pair PSE Conformance Test Suite 5.x.x Tests and Parameters

Parameter	Description	Special Notes	802.3bt Coverage		
Test: det_v			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Open_Circuit_Voc_A=	Peak Open Circuit Detection Voltage on Alt-A Pairset		VOC	PSE6	145.2.5.1
Open_Circuit_Voc_B=	Peak Open Circuit Detection Voltage on Alt-B Pairset		VOC	PSE10	145.2.6.1
Backoff_Voltage_A=	IDLE State voltage during detection backoff on the Alt-A Pairset	*Measured as a minimum voltage in the IDLE region when Dual detection signature is set to 37KΩ*	Voff, VReset	PSE12	145.2.6.2
Backoff_Voltage_B=	IDLE State voltage during detection backoff on the Alt-A Pairset			PSE15	
Backoff_Voltage_Ss=	IDLE State voltage during Single Signature detection backoff across both Pairsets	*Assess the IDLE Backoff voltage a Single Signature PD would see downstream of the full wave bridge with detection signature of 37KΩ. The 802.3bt standard requires PSE to pass through IDLE and separately requires IDLE voltage ≤ 2.8V. The parameter is treated as a Warning (Info mark) only because it is not clear that PSE-PD detection interoperability could be practically be affected by detection signaling that does not drop below 2.8V as a result of invalid detection backoff.*		PSE16 PSE21 PSD75 PSE76	 145.2.7 145.2.10.11
Max_Det_Step_V_A=	Maximum Detection Voltage with Valid Detection Signature - Alt-A Pairset	*Measured with (valid) 26KΩ signature*	Vvalid		
Max_Det_Step_V_B=	Maximum Detection Voltage with Valid Detection Signature - Alt-B Pairset				
Min_Det_Step_V_A=	Minimum Valid Step Voltage with Valid Detection Signature - Alt-A Pairset	*Measured with (valid) 19KΩ signature*			
Min_Det_Step_V_B=	Minimum Valid Step Voltage with Valid Detection Signature - Alt-B Pairset				
Det_Step_Changes_A=	Count of Detection Step Transitions on the Alt-A Pairset	*Measured with (valid) 26KΩ signature*			
Det_Step_Changes_B=	Count of Detection Step Transitions on the Alt-B Pairset				
Min_Step_DV_A=	Detection Step Magnitude from Max Voltage to Min Voltage - Alt-A Pairset	*Measured with (valid) 19KΩ signature*	ΔVtest		
Min_Step_DV_B=	Detection Step Magnitude from Max Voltage to Min Voltage - Alt-A Pairset				
Pre-Det_CC_Step_V_A=	Magnitude of any non-802 pre-detection signaling on the Alt-A Pairset	*Set to 0V if no predetection discovered. Predetection would generally include non-stepped signals that appear on just one pairset at any time.*			
Pre-Det_CC_Step_V_B=	Magnitude of any non-802 pre-detection signaling on the Alt-A Pairset				
Test: det_cc			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Presumed_CC_DET_SEQ=	CC_DET_SEQ as described by the 802.3bt PSE State Machine.	*Based upon observations and analysis of PSE detection and connection check signaling relative to PSE state machine described sequences. Knowledge of this parameter is essential to the evaluation of detection timing behaviors.*	CC_DET_SEQ	PSE2 PSE3 PSE4 PSE7	145.2.4 145.2.5 145.2.5.1
Conn_Chk_SS_V_A=	Peak connection check voltage on the Alt-A Pairset with Single Signature	*These voltages must fall into the valid detection voltage band: 2.8V to 10V.*	Vvalid	PSE20 PSE22	145.2.7
Conn_Chk_SS_V_B=	Peak connection check voltage on the Alt-B Pairset with Single Signature				
Conn_Chk_DS_V_A=	Peak connection check voltage on the Alt-A Pairset with Dual Signature				
Conn_Chk_DS_V_B=	Peak connection check voltage on the Alt-B Pairset with Dual Signature				
High_Signature_CC_A=	Flag indication compliance to PSE state machine on the Alt-A Pairset. 1 is a PASS, 0 is a FAIL.	*The performance of Connection check is insensitive to PD detection signature validity if CC_DET_SEQ = 0, 2, or 3. If CC_DET_SEQ=1, then there should be no Connection Check given an invalid PD signature.*			
High_Signature_CC_B=	Flag indication compliance to PSE state machine on the Alt-B Pairset. 1 is a PASS, 0 is a FAIL.				
4Pair_Start_Fail=	Flag indication that the 4-Pair PSE failed to produce any signaling on at least one Pairset when a valid PD signature was connected.	*This is a serious problem if the PSE is designed to do 4-pair powering.*			
Test: det_i			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Isc_Init_A=	Peak detection current @ >1.5V on the Alt-A Pairset	*PSE's are required to restrict detection current to 5mA or less in order to protect non-PD's. Testing is performed with a large capacitive load and peak current in each voltage band is assess as the derivative of current versus time. The PSA test port signature is visable above ~1.3V.*	Isc	PSE12 PSE17	145.2.6.2
Isc_Init_B=	Peak detection current @ >1.5V on the Alt-B Pairset				
Isc_Det_A=	Peak detection current @ >2.2V on the Alt-A Pairset			PSE21	145.2.7
Isc_Det_B=	Peak detection current @ >2.2V on the Alt-B Pairset				
Det_Slew_A=	Maximum expected detection voltage slew rate on the Alt-A Pairset	*This parameter is derived based upon the peak current and the voltage effect it would have given the minimum PD input capacitance of 0.05 μF on a pairset.*	Vslew		
Det_Slew_B=	Maximum expected detection voltage slew rate on the Alt-B Pairset				
Test: det_time			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Detect_Time_Tdet_A=	Time from start of detection until end of detection on the Alt-A Pairset	*Measurement will include effect of any slow slewing voltages above ~3V on leading and trailing edges of detection*	Tdet	PSE4 PSE5	145.2.5 145.2.5.1
Detect_Time_Tdet_B=	Time from start of detection until end of detection on the Alt-A Pairset				
Backoff_Time_SS=	(IDLE state) Time from end of a detection sequence until start of a new detection sequence given an invalid Single Signature	*PD presents invalid 37KΩ single signature. According to the PSE State Machine, a PSE should pass thorugh IDLE during detection back-off. IDLE is separately described as the voltage band from 0 to 2.8V.*	Tdbo	*PICS as drafted are incomplete here*	
Det2Det_Time=	CC_DET_SEQ 0, 1, and 3 ONLY: The time duration between the end of detection on the PRI Pairset and the start of detection on the SEC pairset.	*Not reported if CC_DET_SEQ= 2*	Tdet2det		
Det+CC_Time=	CC_DET_SEQ 2 ONLY: The total time duration of Detection on both pairsets and Connection Check.	*With CC_DET_SEQ=2, there is no prescribed order or sequence of pairset detections and connection check. The requirement is to complete all in 500msec. The test will relax that requirement in cases where it is observed that at least one connection check and at least one pairset detection are fully completed in the final 500msec that the intent of the 802.3bt standard is accomplished.* *Not Reported if CC_DET_SEQ= 0, 1, or 3.*	Tdet		
CC2Det_Time=	CC_DET_SEQ 0, 3 ONLY: The time from end of Connection Check until start of the first Pairset Detection.	*Not reported if CC_DET_SEQ= 1 or 2.*	Tcc2det		
Test: det_rsource			**802.3 Parm.**	**PIC**	**802.3bt Clause**
PSE_Detect_Source=	PSE Detection Scheme. 0= Voltage probing, 1= Current probing.	*In cases where both current and voltage probing are observed, the report will indicate '1' for current probing.*		*No PICS Coverage*	145.2.6.1
PSE_Source_Zout_A=	The source impedance of the Detection probing on the Alt-A Pairset	*Primarily applicable to current probes that may use series resistance to convert voltage into current. Voltage probing PSE's effectively have zero output impedance and are reported as 0. Current sourcing PSE's should show higher than 45KW unless they deploy a blocking diode to prevent reverse detection by another PSE port.*	Zsource		
PSE_Source_Zout_B=	The source impedance of the Detection probing on the Alt-B Pairset				
Test: det_range			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Rgood_Max_Single=	Maximum Detection signature resistance that gets powered given a Single Signature PD	*Test resolves this to 1KΩ*	Rgood, Rbad	PSE9 PSE11 PSE18 PSE19	145.2.6 145.2.6.1 145.2.6.3 145.2.6.4
Rgood_Min_Single=	Minimum Detection signature resistance that gets powered given a Single Signature PD				
Cgood_Max_Single=	Maximum Capacitive signature that gets powered given a Single Signature PD	*Testing performed with 0.1, 5, 7, and 11 μF capacitive sigantures*	Cgood, Cbad	PSE56	145.2.9
Rgood_Max_Dual_A=	Maximum Detection signature resistance that gets powered on the Alt-A Pairset given a Dual Signature PD	*Test resolves this to 1KΩ*	Rgood, Rbad		
Rgood_Max_Dual_B=	Maximum Detection signature resistance that gets powered on the Alt-B Pairset given a Dual Signature PD				
Rgood_Min_Dual_A=	Minimum Detection signature resistance that gets powered on the Alt-A Pairset given a Dual Signature PD				
Rgood_Min_Dual_B=	Minimum Detection signature resistance that gets powered on the Alt-B Pairset given a Dual Signature PD				
Cgood_Max_Dual_A=	Maximum Capacitive signature that gets powered on the Alt-A Pairset given a Dual Signature PD	*Testing performed with 0.1, 5, 7, and 11 μF capacitive sigantures*	Cgood, Cbad		
Cgood_Max_Dual_B=	Maximum Capacitive signature that gets powered on the Alt-B Pairset given a Dual Signature PD				
Test: cc_response			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Single_Sig_Response=	Flag indicating that the PSE properly characterized a Single Signature PD prior to powering. 1= Success, 0= Failure.	*Testing uses power-ups and subsequence MPS processing to verify correct interpretation of PD siganture type.*		PSE4	145.2.5 145.2.9
Dual_Sig_Response=	Flag indicating that the PSE properly characterized a Dual Signature PD prior to powering. 1= Success, 0= Failure.				
2Pair_PD_A=	Flag indicating the count of Pairsets powered when a valid PD signature is connected only on the Alt-A Pairset. 0= No Pairsets powered, 1= Alt-A Pairset powered, 2= both pairsets powered.	*This test assesses PSE response to a 2-Pair PD connection. In no case should more than one pairset power.*			
2Pair_PD_B=	Flag indicating the count of Pairsets powered when a valid PD signature is connected only on the Alt-BPairset. 0= No Pairsets powered, 1= Alt-A Pairset powered, 2= both pairsets powered.				
Test: class_v			**802.3 Parm.**	**PSE49**	**802.3bt Clause**
Vclass_max_SS=	Maximum Class Event Voltage measured as the peak of both pairsets given a	*Assess with Single Signature adjusted to present 43mA signature for minimum class voltage assessment and 1mA class signature for maximum class voltage assessment.*	Vclass	PSE30 PSE38 PSE40	145.2.8 145.2.8.1
Vclass_min_SS=	Minimum Class Event Voltage measured as the peak of both pairsets given a Single Signature PD emulation				
Vmark_SS=	Median Mark region voltage from the peak of both pairsets given a Single Signature PD emulation	*Measured using a 5mA Mark load current.*	Vmark	PSE42 PSE44	
Vreset_SS=	If the PSE utilizes a Class Probe given Single Signature PD connection, this is the maximum voltage following the completion of the class probe until the start of Event 1 Classification.	*This must drop below 2.8V. Will report as -1 if no Class Probe.*	Vreset	PSE48 PSE49 PSE50	
Vclass_max_DSA=	Maximum Class Event Voltage on the Alt-A Pairset given a Dual Signature PD emulation	*Assess with Dual Signature adjusted to present 43mA signature for minimum class voltage assessment and 1mA class signature for maximum class voltage assessment.*	Vclass	PSE51 PSE52 PSE53	
Vclass_max_DSB=	Maximum Class Event Voltage on the Alt-B Pairset given a Dual Signature PD emulation				
Vclass_min_DSA=	Minimum Class Event Voltage on the Alt-A Pairset given a Dual Signature PD emulation				

Vclass_min_DSB=	Minimum Class Event Voltage on the Alt-B Pairset given a Dual Signature PD emulation				
Vmark_DSA=	Median Mark region voltage on the Alt-A Pairset given a Dual Signature PD emulation	*Measured using a 5mA Mark load current on each pairset.*	Vmark		
Vmark_DSB=	Median Mark region voltage on the Alt-B Pairset given a Dual Signature PD emulation				
Vreset_DSA=	If the PSE utilizes a Class Probe given Dual Signature PD connection, this is the maximum voltage following the completion of the class probe until the start of Event 1 Classification on the Alt-A Pairset.	*This must drop below 2.8V on each pairset. Will report as -1 if no Class Probe.*	Vreset		
Vreset_DSB=	If the PSE utilizes a Class Probe given Dual Signature PD connection, this is the maximum voltage following the completion of the class probe until the start of Event 1 Classification on the Alt- **A** Pairset.				
Test: class_time			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Class_Probe_SS=	Flag indicating if a Class Probe is discovered given a Single Signature PD. 1= Class Probe Discovered, 0= No Class Probe.	*This is informational*		PSE27 PSE29	145.2.8
EV_Count_7_SS=	Class Event Count in response to Class 7 (Single Signature) PD			PSE30	
Long_EV1_Time_SS=	Duration of Event #1 (LCE) Class Pulse prior to power-up given a Single Signature PD connection.		Tlce	PSE31 PSE32	 145.2.8.1
Min_Class_EV_Time_SS=	Minimum duration of any non-LCE Class Event prior to power-up given a Single Signature PD.		Tcev	PSE33 PSE34 PSE35	
Max_Class_EV_Time_SS=	Maximum duration of any non-LCE Class Event prior to power-up given a Single Signature PD.			PSE38 PSE40 PSE43	
Min_Mark_EV_Time_SS=	Minimum duration of any non-final Mark Event prior to power-up given a Single Signature PD.		Tme1	PSE44 PSE50	
Max_Mark_EV_Time_SS=	Maximum duration of any non-final Mark Event prior to power-up given a Single Signature PD.			PSE51 PSE52	
Final_Mark_EV_Time_SS=	Duration of the final Mark Event leading into Power-Up given a Single Signature PD.	*Will be reported as -1 if the PSE fails to apply power.*	Tme2	PSE53	
Cl_Prb_Reset_Time_SS=	If the PSE utilizes a Class Probe given Single Signature PD connection, this is the time duration from end-of-Class-Probe until start of Event #1.		Treset		
Class_Probe_DA=	Flag indicating if a Class Probe is discovered on the Alt-A Pairset given a Dual Signature PD. 1= Class Probe Discovered, 0= No Class Probe.				
EV_Count_5D_DA=	Class Event Count on the Alt-A Pairset in response to a Dual Class 5 PD				
Long_EV1_Time_DA=	Duration of Event #1 (LCE) Class Pulse prior to power-up on the Alt-A Pairset given a Dual Signature PD connection.		Tlce		
Min_Class_EV_Time_DA=	Minimum duration of any non-LCE Class Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.		Tcev		
Max_Class_EV_Time_DA=	Maximum duration of any non-LCE Class Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.				
Min_Mark_EV_Time_DA=	Minimum duration of any non-final Mark Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.		Tme1		
Max_Mark_EV_Time_DA=	Maximum duration of any non-final Mark Event on the Alt-A Pairset prior to power-up given a Dual Signature PD.				
Final_Mark_EV_Time_DA=	Duration of the final Mark Event on the Alt-A Pairset leading into Power-Up given a Dual Signature PD.	*Will be reported as -1 if the PSE fails to apply power.*	Tme2		
Cl_Prb_Reset_Time_DA=	If the PSE utilizes a Class Probe on the Alt-A Pairset given a Dual Signature PD connection, this is the time duration from end-of-Class-Probe until start of Event #1.		Treset		
Class_Probe_DB=	Flag indicating if a Class Probe is discovered on the Alt-B Pairset given a Dual Signature PD. 1= Class Probe Discovered, 0= No Class Probe.				
EV_Count_5D_DB=	Class Event Count on the Alt-B Pairset in response to a Dual Class 5 PD				
Long_EV1_Time_DB=	Duration of Event #1 (LCE) Class Pulse prior to power-up on the Alt-B Pairset given a Dual Signature PD connection.		Tlce		
Min_Class_EV_Time_DB=	Minimum duration of any non-LCE Class Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.		Tcev		
Max_Class_EV_Time_DB=	Maximum duration of any non-LCE Class Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.				
Min_Mark_EV_Time_DB=	Minimum duration of any non-final Mark Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.		Tme1		
Max_Mark_EV_Time_DB=	Maximum duration of any non-final Mark Event on the Alt-B Pairset prior to power-up given a Dual Signature PD.				
Final_Mark_EV_Time_DB=	Duration of the final Mark Event on the Alt-B Pairset leading into Power-Up given a Dual Signature PD.	*Will be reported as -1 if the PSE fails to apply power.*	Tme2		
Cl_Prb_Reset_Time_DB=	If the PSE utilizes a Class Probe on the Alt-B Pairset given a Dual Signature PD connection, this is the time duration from end-of-Class-Probe until start of Event #1.		Treset		
Test: class_response			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Class_3_Count=	Class Event count in response to Class 3 (Single Signature) PD			PSE2	145.2.4
Class_4_Count=	Class Event count in response to Class 4 (Single Signature) PD			PSE4	145.2.5
Class_5_Count=	Class Event count in response to Class 5 (Single Signature) PD			PSE7	145.2.5.1
Class_6_Count=	Class Event count in response to Class 6 (Single Signature) PD			PSE8	145.2.5.4
Class_7_Count=	Class Event count in response to Class 7 (Single Signature) PD	*Should be restricted to 4-Events if Type-3, 5-Events for Type-4*		PSE27 PSE29	145.2.8
Class_8_Count=	Class Event count in response to Class 8 (Single Signature) PD			PSE30	
Class_2D_Count_A=	Class Event count on the Alt-A Pairset in response to a Dual Class 2 PD			PSE31	
Class_2D_Count_B=	Class Event count on the Alt-B Pairset in response to a Dual Class 2 PD			PSE32	145.2.8.1
Class_3D_Count_A=	Class Event count on the Alt-A Pairset in response to a Dual Class 3 PD			PSE33	
Class_3D_Count_B=	Class Event count on the Alt-B Pairset in response to a Dual Class 3 PD			PSE34	
Class_4D_Count_A=	Class Event count on the Alt-A Pairset in response to a Dual Class 4 PD			PSE35	
Class_4D_Count_B=	Class Event count on the Alt-B Pairset in response to a Dual Class 4 PD			PSE36	
Class_5D_Count_A=	Class Event count on the Alt-A Pairset in response to a Dual Class 5 PD	*Should be restricted to 3-Events if Type-3, 4-Events for Type-4*		PSE37	
Class_5D_Count_B=	Class Event count on the Alt-B Pairset in response to a Dual Class 5 PD			PSE41	
Max_SS_Class=	Maximum Single Signature PD Class that the PSE will assign at power-up	*Should be restricted to Class 6 if Type-3, Class 8 if Type-4*			
Max_DS_Class=	Maximum Dual Signature PD Class that both Alt-A and Alt-B Pairsets will assign at power-up	*Should be restricted to Class 4D if Type-3, Class 5D if Type-4*			
Init_Grant_Match=	Flag indicating that the maximum power granted to Dual Signature PD's corresponds to the maximum power granted to Single Signature PD's. 1= Correspondance, 0 = Inconsistent				
2-Pair_Pairset=	Flag indicating which Pairset gets 2-Pair powered if and when the PSE performs 2-Pair powering. Set to 0 if PSE always 4-Pair powers, 1 if Alt-A Pairset powered, 2 if Alt-B Pairset powered.	*Informational*			
PRI_4pr_Pairset=	Primary (PRI) Pairset where Classification occurs given Single Signature PD connection. 1= Alt-A Pairset, 2= Alt-B Pairset, 12= Either Pairset.	*Informational*			
Test: class_err			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Class_Ilim_A=	Classification Event current limit on the Alt-A Pairset.	*PSA test port configured to assure voltage holds above ~14V during these measurements*	Iclass_lim	PSE4 PSE46	145.2.5 145.2.8.1
Class_Ilim_B=	Classification Event current limit on the Alt-B Pairset.			PSE47 PSE48	
Pwr_Cl_52_SS=	Flag indicating if PSE powers a 52mA Class signature given a Single Signature PD. 0= No Power. 1= Power Applied on one pairset. 12= Power Applied on both pairsets.	*PSE's should not power this signature.*			*PICS as drafted are incomplete here*
Pwr_Cl_52_DSA=	Flag indicating if PSE powers the Alt-A Pairset a 52mA Class signature given a Dual Signature PD. 0= No Power. 1= Power Applied.				
Pwr_Cl_52_DSB=	Flag indicating if PSE powers the Alt-B Pairset a 52mA Class signature given a Dual Signature PD. 0= No Power. 1= Power Applied.				
Mark_Ilim_A=	Mark Event current limit on the Alt-A Pairset.		Imark_lim		
Mark_Ilim_B=	Mark Event current limit on the Alt-B Pairset.				
Inval_Sig_EV2_SS=	Flag indicating if the PSE powers an uneven 2-Event classification given a Single Signature PD where Event 1 is 40mA, Event 2 is 18 mA. 0 = No Power, 1= PSE dropped back to 1-event, 2= PSE Powered.	*PSE's should not power these signatures. Set flag to 1 if PSE re-cycles detection and drops back to fewer events in response to uneven signature. That behavior would allow for a legitimate power-up.*			
Inval_Sig_EV4_SS=	Flag indicating if the PSE powers an uneven 4-Event classification given a Single Signature PD where Event #4 differs from Event #3. 0 = No Power, 1= PSE dropped back to 1-3 events, 2= PSE Powered.				
Inval_Sig_EV5_SS=	Flag indicating if the PSE powers an uneven 5-Event classification given a Single Signature PD where Event #5 differs from Event #4. 0 = No Power, 1= PSE dropped back to 1-4 events, 2= PSE Powered.				
Inval_Sig_EV2_DSA=	Flag indicating if the PSE powers the Alt-A Pairset following an uneven 2-Event classification given a Dual Signature PD. 0 = No Power, 1= PSE dropped back to 1-event, 2= PSE Powered.				
Inval_Sig_EV2_DSB=	Flag indicating if the PSE powers the Alt-B Pairset following an uneven 2-Event classification given a Dual Signature PD. 0 = No Power, 1= PSE dropped back to 1-event, 2= PSE Powered.				
Inval_Sig_EV4_DSA=	Flag indicating if the PSE powers the Alt-A Pairset following an uneven 4-Event classification where Event #4 differs from Event #3 given a Dual Signature PD. 0 = No Power, 1= PSE dropped back to 1 -3 events, 2= PSE Powered.				

Inval_Sig_EV4_DSB=	Flag indicating if the PSE powers the Alt-B Pairset following an uneven 4-Event classification where Event #4 differs from Event #3 given a Dual Signature PD. 0 = No Power, 1= PSE dropped back to 1 -3 events, 2= PSE Powered.				
Test: class_lldp			**802.3 Parm.**	**PIC**	**802.3bt Clause**
PSE_LLDP_Time_SS=	Time from Power On to 1st LLDP Frame. -1 = No Frame Received < 45 seconds	*The PSE is required to produce a first 802.3bt or 802.3at TLV within 10 seconds of power-up and link-up by the emulated PD.* *First received frame must match either the 802.3bt or the 802.3at TLV structure. If first received frame is the 802.3at TLV structure, the test will initiate an 802.3bt TLV message and then capture an 802.3bt TLV.*		DLL1 DLL2 DLL3 DLL4 DLL5 DLL7 DLL9 DLL12 PVT3 PVT5 - PVT8 PVT9 - PVT10 PVT11 PVT12 - PVT14 PVT17 PVT18 PVT19 PVT22 PVT25 PVT26 PVT30 PVT38 PVT40 - PVT44	145.5.1 145.5.2 145.5.3 145.5.4 79.3.2 79.3.2.1 79.3.2.2 79.3.2.3 79.3.2.4 79.3.2.5 79.3.2.6 79.3.2.6
LLDP_Length=	TLV Length Field. 29 for 802.3bt				
PSE_Pwr_Pair=	MDI Legacy Powered Pair. Confirm the value of either 1 or 2. All other values fail. Value = 1 means the Signal Pairs are in use. Value = 2 means the Spare Pairs are in use.				
PSE_MDI_Pwr_Sup=	MDI Power Support Field. 4 bit value where bits 0-2 are set and bit 3 is don't care.				
PSE_Pwr_Class=	MDI 802.3at PSE Class Support. Class 4 and above will specify 4				
PSE_Source_Priority=	MDI 802.3at Type-Source-Priority field flag where 0 = VALID entries, 1= INVALID entries. If PSE is Type-3 and Type-4 it must specify Type-2. Power Source can be Primary, Secondary, or Unknown.				
PSE_Ext_Type=	Extended PSE Type. Either Type-3 or Type-4				
PSE_Ext_Status_SS=	Powering Status of PSE. =41 if set to Both_Alts and 4pr_Pwr_Single =21 if et to Alt_A or Alt_B and 2pr_Pwr. Otherwise set to 0.	*Since the Request frame transmitted is from an emulated **Class 8** PD, we should expect that the powering status is 4-Pair powering. If the PSE only does 2-Pair powering at its maximum assigned class, then this is the wrong test suite as the PSE is a 2-Pair PSE. So minimum expected result is '41'.*			
PSE_Ext_Class_SS=	Assigned Class available from the PSE. =41 if Class between 1 and 8 and 4pr_Pwr_Single. =21 if Class between 1 and 4 and 2pr_Pwr. Otherwise set to 0				
PSE_Max_Pwr_SS=	Maximum Port Power Available from the PSE. Valid values are >= 0.1W to <= 99.9W				
PSE_Class_6_Ext_Pwr=	Check if PSE Extends Power beyond Pclass_pd for Class 6. Set to 0 if PSE does NOT extend power and 1 if PSE does extend power	*Only check if PSE_Ext_Class_SS is Class 6 and PSE_Max_Pwr_SS is > 51.0W. Otherwise NOT reported*			
PSE_Pwr_Class_DS=	Value of the Dual-sig Extended Class for Alt-A and Alt-B. Set to 1 if both TLVs are set to Single Signature otherwise set to 0.				
PSE_Echo_Time_1SS=	Time from a PD request for a change to a low power until the frame containing the Echo of that request is received	*Will be reported as -1 if the PSE fails to echo power request*			
PSE_Alloc_Time_1SS=	Time from a PD request for a change to a low power until the frame containing the Allocation of that request is received	*Informational. Will be reported as -1 if the PSE fails to allocate power request.*			
PSE_Alloc_LowPwr_1SS=	Power Allocated by the PSE when requesting a change to a low power				
PSE_Echo_Time_2SS=	Time from a PD request for a change to the max power available until the frame containing the Echo of that request is received	*Will be reported as -1 if the PSE fails echo power request*			
PSE_Alloc_Time_2SS=	Time from a PD request for a change to the max power available until the frame containing the Allocation of that request is received. Will be -1 if allocation never received.	*Informational. Will be reported as -1 if the PSE fails allocate power request.*			
PSE_Alloc_MaxPwr_2SS=	Indicates Power was Allocated by the PSE when requesting a change to the max power available. =1 if Allocated, =0 if Not Allocated				
Link_Down_Shutdown=	Disconnect the LAN. Set to 1 if Power NOT removed. 0 if Power removed				
Test: class_lldp2			**802.3 Parm.**	**PIC**	**802.3bt Clause**
PSE_LLDP_Time_DS=	Time from Power On to 1st LLDP Frame. -1 = No Frame Received < 45 seconds	*The PSE is required to produce a first 802.3bt or 802.3at TLV within 10 seconds of power-up and link-up by the emulated PD.* *First received frame must match either the 802.3bt or the 802.3at TLV structure. If first received frame is the 802.3at TLV structure, the test will initiate an 802.3bt TLV message and then capture an 802.3bt TLV.*		DLL1 DLL2 DLL3 DLL4 DLL5 DLL7 DLL9 DLL12 PVT3 PVT5 - PVT8 PVT9 - PVT10 PVT11 PVT12 - PVT14 PVT17 PVT20 PVT21 PVT25 PVT26 PVT31 PVT34 PVT35 PVT39 PVT40 PVT41	145.5.1 145.5.2 145.5.3 145.5.4 79.3.2 79.3.2.1 79.3.2.2 79.3.2.3 79.3.2.4 79.3.2.6 79.3.2.6
PSE_Ext_Status_DS=	Powering Status of PSE. =42 if set to Both_Alts and 4pr_Pwr_Dual =21 if et to Alt_A or Alt_B and 2pr_Pwr. Otherwise set to 0.	*Since the Request frame transmitted is from an emulated Class 8 PD, we should expect that the powering status is 4-Pair powering. If the PSE only does 2-Pair powering at its maximum assigned class, then this is the wrong test suite as the PSE is a 2-Pair PSE. So minimum expected result is '42'.*			
PSE_Ext_Class_DSA=	Assigned Class available from the PSE on Alt-A. =42 if Class between 1 and 5 and 4pr_Pwr_Dual. =21 if Class between 1 and 4 and 2pr_Pwr. Otherwise set to 0				
PSE_Ext_Class_DSB=	Assigned Class available from the PSE on Alt-B. =42 if Class between 1 and 5 and 4pr_Pwr_Dual. =21 if Class between 1 and 4 and 2pr_Pwr. Otherwise set to 0				
PSE_Max_Pwr_DS=	Maximum Port Power Available from the PSE. Valid values are >= 0.1W to <= 99.9W				
PSE_Pwr_Class_SS=	Value of the Single-sig Extended Class for Alt-A and Alt-B. Set to 1 if TLV is set to Single Signature otherwise set to 0.				
PSE_Echo_Time_1DS=	Time from a PD request for a change to a low power until the frame containing the Echo of that request is received	*Will be reported as -1 if the PSE fails to echo both pairset power requests*			
PSE_Alloc_Time_1DS=	Time from a PD request for a change to a low power until the frame containing the Allocation of that request is received	*Informational - Will be reported as -1 if the PSE fails to allocated both pairset power requests*			
PSE_Alloc_LowPwr_1DSA=	Power Allocated on Alt-A by the PSE when requesting a change to a low power				
PSE_Alloc_LowPwr_1DSB=	Power Allocated on Alt-B by the PSE when requesting a change to a low power				
PSE_Echo_Time_2DS=	Time from a PD request for a change to the max power available until the frame containing the Echo of that request is received	*Will be reported as -1 if the PSE fails to echo both pairset power requests*			
PSE_Alloc_Time_2DS=	Time from a PD request for a change to the max power available until the frame containing the Allocation of that request is received	*Informational - Will be reported as -1 if the PSE fails to allocated both pairset power requests*			
PSE_Alloc_MaxPwr_2DSA=	Indicates Power was Allocated on Alt-A by the PSE when requesting a change to the max power available. =1 if Allocated, =0 if Not Allocated				
PSE_Alloc_MaxPwr_2DSB=	Indicates Power was Allocated on Alt-B by the PSE when requesting a change to the max power available. =1 if Allocated, =0 if Not Allocated				
PSE_Alloc_Limit_DS=	PSE does not allocate more than the Class assigned at Power-Up. =1 if PSE Limits power Allocation, =0 if PSE does not	*Class at Power-Up determined by the min of PD Requested Class and PSE Assigned Class*			
Test: pwrup_time			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Pwr_On_Time_Tpon_SS=	Time duration from the end of Detection and Connection Check until the end of the POWER_UP state given a Single Signature PD.	*The end of POWER_UP state is assessed as Tinrush_min (50 msec) following the observed Power-Up. If one pairset powering is staggered, then measurement is performed using the first pairset powered.* *The minimum expected Tpon is Tlce_min (88msec)+Tme2_min (6msec)+Tinrush_min (50 msec) = 144msec.*	Tpon	PSE4 PSE80 PSE81 *PICS as drafted are incomplete here*	145.2.5 145.2.10.14
Pwr_On_Time_Tpon_DSA=	Time duration from the end of Detection and Connection Check until the end of the POWER_UP state on the Alt-A Pairset given a Dual Signature PD.				
Pwr_On_Time_Tpon_DSB=	Time duration from the end of Detection and Connection Check until the end of the POWER_UP state on the Alt-B Pairset given a Dual Signature PD.				
Pwrup_Rise_Time_A=	Estimated time (μsec) for the Alt-A Pairset to transit from 10% of Vpse to 90% of Vpse while applying power.	*Measurement is performed with minimal load current (~0mA) during the power-up.* *Fastest rise time that can be measured is 6usec. If -99, then rise time measurement likely false triggered on a large voltage transient most likely at start or end of classification pulse.* *As of report version **5.1.07**, this parameter is PASS/**INFO** and not PASS/**FAIL** because technically speaking, the explicit measurement of 10% to 90% of **Vpse** is not possible with the PSA time interval measurement and is not feasible using any method since the 802.3bt PSE powers up from Vmark (2-Event classification). A rise time measurement with an **INFO** mark indicates a power-up slew rate that exceeds the 'intent' of the 802.3 standard.*	Trise		
Pwrup_Rise_Time_B=	Estimated time (μsec) for the Alt-B Pairset to transit from 10% of Vpse to 90% of Vpse while applying power.				
Pwr_Stagger_Time_SS4=	Time duration between primary (PRI) Pairset power-up and secondary (SEC) pairset power-up given Single Signature Class 4. Set to 0 for simultaneous power-ups and to -1 for 2-pair power-ups.				
Pwr_Stagger_Time_SS5=	Time duration between primary (PRI) Pairset power-up and secondary (SEC) pairset power-up given Single Signature Class 5. Set to 0 for simultaneous power-ups and to -1 for 2-pair power-ups.	*PSE must have both pairsets powered within ~75 msec of each other. 2-Pair power-ups not allowed.*			
Pwr_Stagger_Time_DS=	Time duration between primary (PRI) Pairset power-up and secondary (SEC) pairset power-up given Dual Signature PD. Set to 0 for simultaneous power-ups and to -1 for 2-pair power-ups.	*Informational*			
Test: pwrup_inrush			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Iinrush_min_Class_3=	Minimum 4-Pair Inrush current from power-up until 50msec after power-up given Single Signature Class 3 PD	*All testin performed with foldback suppression to maintain minimum port voltage > 30V while PSE is in current limiting state.*	Iinrush	PSE4 PSE68 PSE69	145.2.5 145.2.10.7
Iinrush_min_Class_5=	Minimum 4-Pair Inrush current from power-up until 50msec after power-up given Single Signature Class 5 PD				
Iinrush_min_Class_7=	Minimum 4-Pair Inrush current from power-up until 50msec after power-up given Single Signature Class 7 PD				
Iinrush_min_Class_1D_A=	Minimum Alt-A Pairset Inrush current from power-up until 50msec after power-up given Dual Signature Class PD		Inrush_2p		
Iinrush_min_Class_1D_B=	Minimum Alt-B Pairset Inrush current from power-up until 50msec after power-up given Dual Signature Class PD				
Iinrush_4P_max_Class_3=	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 3 PD		Iinrush		

Iinrush_4P_max1_Class_5=	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 5 PD and given a PSE that grants a maximum of Class 4 power.				
Iinrush_4P_max2_Class_5=	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 5 PD and given a PSE that grants greater than Class 4 power.				
Iinrush_4P_max1_Class_7=	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants a maximum of Class 4 power.				
Iinrush_4P_max2_Class_7=	Maximum 4-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants greater than Class 4 power.				
Iinrush_2P_max_Class_3=	Maximum 2-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 3 PD.		Inrush_2p		
Iinrush_2P_max1_Class_7=	Maximum 2-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants a maximum of Class 4 power.				
Iinrush_2P_max2_Class_7=	Maximum 2-Pair Inrush current from 1msec after power-up until shutdown given a Single Signature Class 7 PD and given a PSE that grants greater than Class 4 power.				
Iinrush_2p_max_Cl_1D_A=	Maximum 2-Pair Inrush current on the Alt-A Pairset from 1msec after power-up until shutdown given a Dual Signature Class 1 PD.				
Iinrush_2p_max_Cl_1D_B=	Maximum 2-Pair Inrush current on the Alt-B Pairset from 1msec after power-up until shutdown given a Dual Signature Class 1 PD.				
Tinrush_minPr_Class_3=	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 3 PD - minimum of the Alt-A and Alt-B Pairsets	*If only one pairset powers, use the same figure for minPr and maxPr parameters*	Tinrush		
Tinrush_maxPr_Class_3=	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 3 PD - maximum of the Alt-A and Alt-B Pairsets				
Tinrush_minPr_Class_7=	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 7 PD - minimum of the Alt-A and Alt-B Pairsets				
Tinrush_maxPr_Class_7=	Inrush Shutdown Time measured from power-up until power removal given Single Signature Class 7 PD - maximum of the Alt-A and Alt-B Pairsets				
Tinrush_Class_1D_A=	Inrush Shutdown Time measured from power-up until power removal on the Alt-A Pairset given Dual Signature Class 1 PD				
Tinrush_Class_1D_B=	Inrush Shutdown Time measured from power-up until power removal on the Alt-B Pairset given Dual Signature Class 1 PD				
Delay_Inrush_Class_7=	Inrush Shutdown Time measured from power-up until power removal on both Pairsets given a Single Signture Class 7 PD and an inrush overload that is delayed by 25msec from power-up				
Delay_Inrush_Class_2D_A=	Inrush Shutdown Time measured on the Alt-A Pairset from power-up until power removal given a Dual Signture Class 1 PD and an inrush overload that is delayed by 25msec from power-up of the Alt-A Pairset				
Delay_Inrush_Class_2D_B=	Inrush Shutdown Time measured on the Alt-B Pairset from power-up until power removal given a Dual Signture Class 1 PD and an inrush overload that is delayed by 25msec from power-up of the Alt-B Pairset				
45ms_Pwr_Stat_Class_7=	Flag indicating if PSE maintained power when a 45msec Inrush current overload is applied given a Single Signature Class 7 PD. 1= Power Maintained, 0= Power Removed.				
45ms_Pwr_Stat_Class_2D_A=	Flag indicating if PSE maintained power on the Alt-A Pairset when a 45msec Inrush current overload is applied given a Dual Signature Class 2 PD. 1= Power Maintained, 0= Power Removed.				
45ms_Pwr_Stat_Class_2D_B=	Flag indicating if PSE maintained power on the Alt-B Pairset when a 45msec Inrush current overload is applied given a Dual Signature Class 2 PD. 1= Power Maintained, 0= Power Removed.				
Vinrush_Class_2D_A=	Inrush voltage on the Alt-A Pairset while the PSE is in current limit.	*Informational - should be > 30V*	Inrush		
Vinrush_Class_2D_B=	Inrush voltage on the Alt-B Pairset while the PSE is in current limit.				
Test: pwron_v			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Vpse_Max_Alt_A=	PSE output voltage on the Alt-A Pairset when PSE is powered and lightly loaded (~1W).		Vport_pse_2p	PSE57 PSE58	145.2.10 145.2.10.1
Vpse_Max_Alt_B=	PSE output voltage on the Alt-B Pairset when PSE is powered and lightly loaded (~1W).			PSE61 PSE64	145.2.10.3 145.2.10.5
Vpse_Min_Alt_A=	PSE output voltage on the Alt-A Pairset when PSE is powered and heavily loaded (~95% of **Pclass**).				
Vpse_Min_Alt_B=	PSE output voltage on the Alt-B Pairset when PSE is powered and heavily loaded (~95% of **Pclass**).				
Vport_PSE_diff=	Difference between Alt-A and Alt-B output voltages when PSE is 4-pair powered and has zero mA load.	*Very challenging to meter this to the 10 mV required by the specification! Absolute accuracy of PSA test port DC meter will allow for up to 750 mV meter disagreement between pairsets though "Typical" is more likely on the order of 200mV range.*	Vport_pse_diff		
V_ripple_A=	Low frequency (20Hz-150Hz) ripple measured on the Alt-A Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.	*AC peak-peak measurements are made with a PoE load capacitance of 0.05 μF as this is the minimum possible input capacitance a PD will connect while PSE port is powered.*	Vnoise		
V_ripple_B=	Low frequency (20Hz-150Hz) ripple measured on the Alt-B Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.				
V_noise_A=	High frequency (50KHz-300KHz) noise measured on the Alt-A Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.				
V_noise_B=	High frequency (50KHz-300KHz) noise measured on the Alt-B Pairset when the PSE is powered. Measurement made at both low and high power load with maximum of the two reported.				
V_trans_A=	Minimum voltage mesured on the Alt-A Pairset during a load transition from ~0.5W to ~**Pclass** and back over a short (< 5msec) duration.		Vtran_2p		
V_trans_B=	Minimum voltage mesured on the Alt-B Pairset during a load transition from ~0.5W to ~**Pclass** and back over a short (< 5msec) duration.				
Test: pwron_pwrcap			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Max_Asgn_Class_SS=	The maximum classification a PSE will assign to a Single Signature PD through either event counts or LLDP.	This governs the minimum power the PSE is required to source to all Single Signature PD's.		PSE60 PSE65	145.2.10.1 145.2.10.6
Pcon_c1=	Maximum sustained power (in watts) to a Class 1 PD	*Maximum sustained power must equal or exceed **Pclass** as defined in 802.3bt. **Pclass** is dependent on:* *1. Number of powered pairs* *2. PSE output voltage **Vpse** under load* *3. PSE assigned class (that is the minimum of **PD Class** and **Max_Asgn_Class_SS**)* ***Icon_%_cX** is a ratio of the measured maximum sustained load current to **Icon** that is **Pclass** / **Vpse**. Like **Pclass**, **Icon** is limited by **Max_Asgn_Class_SS** in power demoted situations.*	Icon	PSE82 *PICS as drafted are incomplete here*	145.2.11
Icon_%_c1=	Maximum sustained load current as a % of **Icon** for a Class 1 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c2=	Maximum sustained power (in watts) to a Class 2 PD				
Icon_%_c2=	Maximum sustained load current as a % of **Icon** for a Class 2 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c3=	Maximum sustained power (in watts) to a Class 3 PD				
Icon_%_c3=	Maximum sustained load current as a % of **Icon** for a Class 3 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c4=	Maximum sustained power (in watts) to a Class 4 PD				
Icon_%_c4=	Maximum sustained load current as a % of **Icon** for a Class 4 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c5=	Maximum sustained power (in watts) to a Class 5 PD				
Icon_%_c5=	Maximum sustained load current as a % of **Icon** for a Class 5 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c6=	Maximum sustained power (in watts) to a Class 6 PD				
Icon_%_c6=	Maximum sustained load current as a % of **Icon** for a Class 6 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c7=	Maximum sustained power (in watts) to a Class 7 PD				
Icon_%_c7=	Maximum sustained load current as a % of **Icon** for a Class 7 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Pcon_c8=	Maximum sustained power (in watts) to a Class 8 PD				
Icon_%_c8=	Maximum sustained load current as a % of **Icon** for a Class 8 PD, the minimum required load current associated with **Pclass**. To pass, this should be ≥ 100%.				
Type_N_Enable=	Powering status when a load of ~ 90% **Pclass** (Icon) is applied at 80 msec following power-up.	*= 1 if PHY granting PSE maintains power or if an LLDP granting PSE removes power* *= 0 if PHY granting PSE removes power or if an LLDP granting PSE maintains power*	Tdelay (PD)		
Pclass_LLDP_95%=	LLDP Granting PSE's Only: Power status when a negotiation for 95% of the	*The Pclass_pd value associated with the 95% (or 75%) maximum power grant is computed, then from that and the PSE voltage, the PSE load is computed and applied following the LLDP negotiation.*	Pclass		
Pclass_LLDP_75%=	LLDP Granting PSE's Only: Power status when a negotiation for 75% of the maximum available PSE port power is negotiated, then the corresponding PD load with maximum cable loss is applied.				

Max_Asgn_Class_DS=	The maximum classifications a PSE will assign to a Dual Signature PD (on both pairsets) through either event counts or LLDP.	*This governs the minimum power the PSE is required to source on both pairsets to all Dual Signature PD's.*			
Pcon_c1DA=	Maximum sustainded power on the Alt-A pairset (in watts) to a Dual Class 1 PD	*Maximum sustained power must equal or exceed **Pclass_2p** as defined in 802.3bt. **Pclass_2p** is dependent on:* *1. PSE pairset output voltage **Vpse** under load* *2. PSE assigned class (that is the minimum of **PD Class** and **Max_Asgn_Class_DS**)* *Icon_%_cXDA abd Icon_%_cXDB are ratios of the measured maximum sustained pairset load current to **Icon_2p** that is **Pclass_2p** / **Vpse**. Like **Pclass_2p**, **Icon_2p** is limited by **Max_Asgn_Class_DS** in power demoted situations.* *The test will respond to single-pairset power-ups for Non-LLDP granting PSE's when emulated class exceeds the maximum assigned class that would be granted to both pairsets. In this case, it will test just the powered pairset to the assigned class on that pairset.*	Icon_2p		
Icon_%_c1DA=	Given a Dual Class 1 PD, the maximum sustained Alt-A load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.				
Pcon_c2DB=	Maximum sustainded power on the Alt-B pairset (in watts) to a Dual Class 2 PD				
Icon_%_c2DB=	Given a Dual Class 2 PD, the maximum sustained Alt-B load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.				
Pcon_c3DA= OR Pcon_c3DB=	Maximum sustainded power on the Alt-A pairset (or Alt-B if only Alt-B powers) in watts to a Dual Class 3 PD				
Icon_%_c3DA= OR Icon_%_c3DB=	Given a Dual Class 3 PD, the maximum sustained Alt-A (or Alt-B if only Alt-B powers) load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.				
Pcon_c4DA= OR Pcon_c4DB=	Maximum sustainded power on the Alt-A pairset (or Alt-B if only Alt-B powers) in watts to a Dual Class 4 PD				
Icon_%_c4DA= OR Icon_%_c4DB=	Given a Dual Class 4 PD, the maximum sustained Alt-A (or Alt-B if only Alt-B powers) load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.				
Pcon_c4DA= OR Pcon_c4DB=	Maximum sustainded power on the Alt-A pairset (or Alt-B if only Alt-B powers) in watts to a Dual Class 5 PD				
Icon_%_c5DA= OR Icon_%_c5DB=	Given a Dual Class 5 PD, the maximum sustained Alt-A (or Alt-B if only Alt-B powers) load current as a % of **Icon_2p**, the minimum required load current associated with **Pclass_2p**. To pass, this should be ≥ 100%.				
Test: pwron_unbal			**802.3 Parm.**	**PIC**	**802.3bt Clause**
pseP2pUnbal_c4A=	If a PSE powers Class 4 with 4-Pairs: The powering status when a total load of ~90% Icon is shifted onto the Alt-A pairset and the load current on the Alt-B pairset is zero mA.	*If the PSE powers with just 2 pairs, set to -1. If 4-Pair powered PSE tolerates the load unbalance, set to 1. Otherwise, set to 0.*	Icon_2p_unb	*PICS as drafted are incomplete here*	145.2.10 145.2.10.6.1
pseP2pUnbal_c4B=	If a PSE powers Class 4 with 4-Pairs: The powering status when a total load of ~90% Icon is shifted onto the Alt-B pairset and the load current on the Alt-A pairset is zero mA.				
pseP2pUnbal_c5A= pseP2pUnbal_c6A= pseP2pUnbal_c7A= pseP2pUnbal_c8A=	The powering status when a total load of ~90% **Icon** is split such that the Alt-A pairset gets **Icon_2p_unb** and the Alt-B pairset gets the remaining load current (90% * **Icon** - **Icon_2p_unb**). **Icon_2p_unb** = 560mA for assigned class 5, 692mA for assigned class 6, 794mA for assigned class 7, and 948mA for assigned class 8.	*As described above, **Icon** is determined as a function of:* *1. PSE output voltage **Vpse** under load* *2. PSE assigned class (that is the minimum of **PD Class** and **Max_Asgn_Class_SS**)*			
pseP2pUnbal_c5B= pseP2pUnbal_c6B= pseP2pUnbal_c7B= pseP2pUnbal_c8B=	The powering status when a total load of ~90% **Icon** is split such that the Alt-B pairset gets **Icon_2p_unb** and the Alt-A pairset gets the remaining load current (90% * **Icon** - **Icon_2p_unb**). **Icon_2p_unb** = 560mA for assigned class 5, 692mA for assigned class 6, 794mA for assigned class 7, and 948mA for assigned class 8.				
Test: pwron_maxi			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Ilim_2p_max_SSA= Ilim_2p_max_SSB=	Maximum current measured during short circuit overload from $pseMaxClass_SS PD on Alt-A and Alt-B pairsets.		Ilim_2p	PSE61 PSE71 PSE72 PSE73 PSE79	145.2.10.3 145.2.10.9 145.2.10.13
Tlim_SS=	Time from short circuit overload assertion until first pairset shutdown.	***Tlim**, while specified, is not a practically enforceable parameter because of clause 145.2.10.9 that says that a PSE can remove power without regard to **Tlim** if the voltage drops below **Vport_pse**(min). A PSE in current limit will, as a practical matter, always have a sub **Vport_pse**(min) voltage.*	Tlim		
Ilim_2p_max_DSA= Ilim_2p_max_DSB=	Maximum current measured during short circuit overload from $pseMaxClass_DS PD on Alt-A and Alt-B pairsets.		Ilim_2p		
Tlim_DSA= Tlim_DSB=	Time from short circuit overload assertion until Alt-A pairset shutdown. Time from short circuit overload assertion until Alt-B pairset shutdown.	*See comment above.*	Tlim		
Ilim_min_cAB3=	Minimum current sustained with **Ilim_min_2p** (400mA) applied Alt-A, then Alt-B pairsets for **Tlim_min**	***Ilim_min** current loads applied to one pairset at a time*	Ilim_2p(min), Tlim(min)		
Max_trans_c3=	PSE Powering status at end of the Class 3 Peak Transient traces	*Should be powered. 1= Powered, 0= Down, -1= Never Powered*			
Ilim_min_cAB4=	Minimum current sustained with **Ilim_min_2p** (684mA) applied Alt-A, then Alt-B pairsets for **Tlim_min**	*Ilim_min current loads applied to one pairset at a time*			
Max_trans_c4=	PSE Powering status at end of the Class 4 Peak Transient traces	*Should be powered. 1= Powered, 0= Down, -1= Never Powered*			
Ilim_min_cAB5=	Minimum current sustained with **Ilim_min_2p** (580mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c5=	PSE Powering status at end of the Class 5 Peak Transient traces	*Should be powered. 1= Powered, 0= Down*			
Ilim_min_cAB6=	Minimum current sustained with **Ilim_min_2p** (720mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c6=	PSE Powering status at end of the Class 6 Peak Transient traces	*Should be powered. 1= Powered, 0= Down*			
Ilim_min_cAB7=	Minimum current sustained with **Ilim_min_2p** (850mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c7=	PSE Powering status at end of the Class 7 Peak Transient traces	*Should be powered. 1= Powered, 0= Down*			
Ilim_min_cAB8=	Minimum current sustained with **Ilim_min_2p** (1005mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c8=	PSE Powering status at end of the Class 8 Peak Transient traces	*Should be powered. 1= Powered, 0= Down*			
Ilim_min_cAB3D=	Minimum current sustained with **Ilim_min_2p** (400mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c3D=	PSE Powering status at end of the Dual Signature Class 3 Peak Transient traces	*Should be powered. 1= Powered, 0= Alt-A or Alt-B Down*			
Ilim_min_cAB4D=	Minimum current sustained with **Ilim_min_2p** (684mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c4D=	PSE Powering status at end of the Dual Signature Class 3 Peak Transient traces	*Should be powered. 1= Powered, 0= Alt-A or Alt-B Down*			
Ilim_min_cAB5D=	Minimum current sustained with **Ilim_min_2p** (990mA) applied Alt-A and Alt-B pairsets for **Tlim_min**	*Ilim_min applied concurrently to both pairsets*			
Max_trans_c5D=	PSE Powering status at end of the Dual Signature Class 3 Peak Transient traces	*Should be powered. 1= Powered, 0= Alt-A or Alt-B Down*			
Vtrans_2p_A=	Minimum Alt-A voltage in response to a maximum transient overload (Ilim_min) of 250usec duration from the maximum class PD a PD will support		Vtran_2p		
Vtrans_2p_B=	Minimum Alt-B voltage in response to a maximum transient overload (Ilim_min) of 250usec duration from the maximum class PD a PD will support				
Iport_max_type3=	Flag indicating power removed from both pairsets of Type-3 PSE with 852mA per pairset for > 75 msec		Iport_2p		
Iport_max_type4=	Flag indicating power removed from both pairsets of Type-4 PSE with 1302mA per pairset for > 75 msec				
Ilps_type4=	Flag indicating power removed from both pairsets of Type-4 PSE with Maximum LPS current per pairset for > 4 sec	*Maximum LPS current is 100W / Vpse*	Ilps_2p		
Test: pwron_overId			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Ipeak_c1=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 1 PD	*1 = Power Maintained* *0 = Power Dropped* *Ipeak determined based on Vpse, Ppeak_pd, and Rchan*	Ipeak	PSE62 PSE66 PSE82 *PICS as drafted are incomplete here*	145.2.10.3 145.2.10.6 145.2.11
Ipeak_c2=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 2 PD				
Ipeak_c3=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 3 PD				
Vport_Ipeak_c3=	Minimum voltage during **Ipeak** Class 3 transient	*Should be in the range of Vpse for Type-3/4 PSE*	Vport_pse		
Ipeak_5%DC_c3=	Flag indicating if PSE maintains powwer following a 5% duty cylcle transient load of **Ipeak** to a Class 3 PD	*1 = Power Maintained* *0 = Power Dropped*			
Ipeak_c4=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 4 PD	*See Ipeak_c3 above*	Ipeak		
Vport_Ipeak_c4=	Minimum voltage during **Ipeak** Class 4 transient	*Should be in the range of Vpse for Type-3/4 PSE*	Vport_pse		
Ipeak_5%DC_c4=	Flag indicating if PSE maintains powwer following a 5% duty cylcle transient load of **Ipeak** to a Class 4 PD	*1 = Power Maintained* *0 = Power Dropped*			
Ipeak_c5=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 4 PD	*See Ipeak_c3 above*	Ipeak		
Vport_Ipeak_c5=	Minimum voltage during **Ipeak** Class 5 transient	*Should be in the range of Vpse for Type-3/4 PSE*	Vport_pse		
Ipeak_5%DC_c5=	Flag indicating if PSE maintains powwer following a 5% duty cylcle transient load of **Ipeak** to a Class 4 PD	*1 = Power Maintained* *0 = Power Dropped*			
Ipeak_c6=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 6 PD	*See Ipeak_c3 above*	Ipeak		
Vport_Ipeak_c6=	Minimum voltage during **Ipeak** Class 6 transient	*Should be in the range of Vpse for Type-3/4 PSE*	Vport_pse		
Ipeak_5%DC_c6=	Flag indicating if PSE maintains powwer following a 5% duty cylcle transient load of **Ipeak** to a Class 6 PD	*1 = Power Maintained* *0 = Power Dropped*			
Ipeak_c7=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 7 PD	*See Ipeak_c3 above*	Ipeak		
Vport_Ipeak_c7=	Minimum voltage during **Ipeak** Class 7 transient	*Should be in the range of Vpse for Type-4 PSE*	Vport_pse		

Ipeak_5%DC_c7=	Flag indicating if PSE maintains powwer following a 5% duty cylcle transient load of **Ipeak** to a Class 7 PD	*1 = Power Maintained* *0 = Power Dropped*			
Ipeak_c8=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Class 8 PD	*See Ipeak_c3 above*	Ipeak		
Vport_Ipeak_c8=	Minimum voltage during **Ipeak** Class 8 transient	*Should be in the range of Vpse for Type-4 PSE*	Vport_pse		
Ipeak_5%DC_c8=	Flag indicating if PSE maintains powwer following a 5% duty cylcle transient load of **Ipeak** to a Class 8 PD	*1 = Power Maintained* *0 = Power Dropped*			
Ipeak_c1D=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Dual Class 1 PD	*See Ipeak_c3 above*	Ipeak_2p		
Ipeak_c2D=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Dual Class 2 PD				
Ipeak_c3D=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Dual Class 3 PD				
Ipeak_c4D=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Dual Class 4 PD				
Ipeak_c5D=	Flag indicating if the PSE maintains power following an **Ipeak** current transient of duration **Tcut_min** (50msec) to a Dual Class 5 PD				
Test: mps_dc_valid			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Ihold_c3=	Minimum 4-pair load current, split evently between pairsets, that will maintain power to a Class 3 PD		Ihold	PSE83 PSE84	145.2.12
Ihold_2p_c3A=	Minimum 2-pair load current on Alt-A pairset that will maintain power to a Class 3 PD. If PSE powers with 4-pairs, the Alt-B pairset will be drawing 1.5 mA during the scan.	*With 4-pair powering, the test evaluates if pairset current impacts disconnect shutdown. If PSE uses primarily the 4-pair **Ihold** to decide, then **Ihold_2p_c3** will generally report top-of-the-range 5mA. **Ihold_2p_c3** must report in the band of 2mA to 5mA.* *With 2-pair powering, the test simply determines the minimum 2-pair current that maintains power.* *PSE's that rapidly convert from 4-Pair to 2-Pair powering during Tmpdo will report as '-1'.*	Ihold_2p	PSE85 PSE87 PSE88 PSE91 PSE93 PSE96	
Ihold_2p_c3B=	Minimum 2-pair load current on Alt-B pairset that will maintain power to a Class 3 PD. If PSE powers with 4-pairs, the Alt-A pairset will be drawing 1.5 mA during the scan.				
Ihold_c5=	Minimum 4-pair load current, split evently between pairsets, that will maintain power to a Class 5 PD		Ihold		
Ihold_2p_c5A=	Minimum 2-pair load current on Alt-A pairset that will maintain power to a Class 5 PD when the Alt-B pairset is drawing 1.5 mA	*Test evaluates if pairset current impacts disconnect shutdown. If PSE uses primarily the 4-pair **Ihold** to decide, then **Ihold_2p_c5** will generally report top-of-the-range 7mA. **Ihold_2p_c5** must report in the band of 2mA to 7mA.*	Ihold_2p		
Ihold_2p_c5B=	Minimum 2-pair load current on Alt-B pairset that will maintain power to a Class 5 PD when the Alt-A pairset is drawing 1.5 mA				
Ihold_c7=	Minimum 4-pair load current, split evently between pairsets, that will maintain power to a Class 7 PD		Ihold		
Ihold_2p_c7A=	Minimum 2-pair load current on Alt-A pairset that will maintain power to a Class 7 PD when the Alt-B pairset is drawing 1.5 mA	*Test evaluates if pairset current impacts disconnect shutdown. If PSE uses primarily the 4-pair **Ihold** to decide, then **Ihold_2p_c7** will generally report top-of-the-range 7mA. **Ihold_2p_c7** must report in the band of 2mA to 7mA.*	Ihold_2p		
Ihold_2p_c7B=	Minimum 2-pair load current on Alt-B pairset that will maintain power to a Class 7 PD when the Alt-A pairset is drawing 1.5 mA				
Ihold_2p_c2DA=	Minimum Alt-A load current to maintain power on the Alt-A pairset given a dual signature PD and 80mA load on the Alt-B pairset.		Ihold_2p		
Ihold_2p_c2DB=	Minimum Alt-B load current to maintain power on the Alt-B pairset given a dual signature PD and 80mA load on the Alt-A pairset.				
LP_MPS_Tol_c3=	Flag indicating if 2-Pair or 4-Pair power is maitained following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 3 PD.	*1= Power Maintained* *0= Power Dropped*	Tmps, Tmpdo(min), Ihold(max)		
LP_MPS_Tol_c5=	Flag indicating if 4-Pair power is maitained following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 5 PD.				
LP_MPS_Tol_c7=	Flag indicating if 4-Pair power is maitained following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 7 PD.				
LP_MPS_Tol_c2D=	Flag indicating if power is maitained on both pairsets following a succession of low power MPS impulses providing valid current for Tmps with 2.15% duty cycle given a Class 2D PD.				
Test: mps_dc_pwrdn			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Tmpdo_c3A=	Time from PD disconnect until power removal on Alt-A pairset given a Class 3 PD. Tested using a load current of **Ihold_min** - 1 mA.	*Will report 9999 if power is not removed.*	Tmpdo, Ihold(min), Ihold_2p(min)	PSE83 PSE85 PSE86 PSE89 PSE90 PSE92 PSE94 PSE95	145.2.12
Tmpdo_c3B=	Time from PD disconnect until power removal on Alt-B pairset given a Class 3 PD. Tested using a load current of **Ihold_min** - 1 mA.				
Tmpdo_c5A=	Time from PD disconnect until power removal on Alt-A pairset given a Class 5 PD. Tested using a load current of **Ihold_min** - 1 mA.				
Tmpdo_c5B=	Time from PD disconnect until power removal on Alt-B pairset given a Class 5 PD. Tested using a load current of **Ihold_min** - 1 mA.				
Tmpdo_c7A=	Time from PD disconnect until power removal on Alt-A pairset given a Class 7 PD. Tested using a load current of **Ihold_min** - 1 mA.				
Tmpdo_c7B=	Time from PD disconnect until power removal on Alt-B pairset given a Class 7 PD. Tested using a load current of **Ihold_min** - 1 mA.				
Tmpdo_c2DA=	Time from Alt-A pairset disconnect until power removal on the Alt-A pairset given a dual Class 2 PD. Tested using load current of **Ihold_2p_min** - 1 mA.				
4pr_Stat_c2DA=	Flag indicating if PSE removes power on one pairset or both pairsets when the Alt-A pairset is disconnected.	*0 = Both pairsets shut down* *2 = Alt-A pairset not shut down* *1 = Only Alt-A pairset shut down*			
Tmpdo_c2DB=	Time from Alt-B pairset disconnect until power removal on the Alt-B pairset given a dual Class 2 PD. Tested using load current of **Ihold_2p_min** - 1 mA.	*Will report 9999 if power is not removed.*	Tmpdo, Ihold(min), Ihold_2p(min)		
4pr_Stat_c2DB=	Flag indicating if PSE removes power on one pairset or both pairsets when the Alt-B pairset is disconnected.	*0 = Both pairsets shut down* *2 = Alt-B pairset not shut down* *1 = Only Alt-B pairset shut down*			
Test: pwrdn_time			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Turnoff_time_Toff_A=	PSE shutdown time on the Alt-A pairset following a PD Disconnect. Test is performed with a 320KΩ load appllied across the pairset.	*This test performs measurements of two disconnect shutdowns, one with a fixed discharge current applied, in order to establish the discharge time constant (RC), then the output capacitance **Cout**, then the passive discharge resistance, **Rp**. Using these circuit parameters, the test computes **Toff** by connecting a virtual 320KΩ resistance to each pairset output. Bot **Cout** and **Rp** are corrected for parasitic test port elements.*	Toff	PSE74	145.2.10.10
Turnoff_time_Toff_B=	PSE shutdown time on the Alt-B pairset following a PD Disconnect. Test is performed with a 320KΩ load appllied across the pairset.				
Cout_A=	PSE output capacitance on the Alt-A pairset as measured immediately after disconnect shutdown.		Cout	PSE14	145.2.6.1
Cout_B=	PSE output capacitance on the Alt-B pairset as measured immediately after disconnect shutdown.				
Output_Rp_A=	Effective PSE discharge resistance on the Alt-A pairset as measured immediately after disconnect shutdown.				
Output_Rp_B=	Effective PSE discharge resistance on the Alt-B pairset as measured immediately after disconnect shutdown.				
Test: pwrdn_v			**802.3 Parm.**	**PIC**	**802.3bt Clause**
Error_Delay_SS_A=	Time between overload shutdown and attempted new detection of a single signature PD on the Alt-A pairset.	*Following an error condition such as an overload shutdown, the PSE is required to wait at least 750msec before "attempting to power" a PD.* *Clause 145.2.10.11 requires the PSE to be in the Voff band (0-2.8V) during the ERROR_DELAY state in the PSE state machine.*	Ted	PSE4 PSE57	145.2.10.15
Error_Delay_SS_B=	Time between overload shutdown and attempted new detection of a single signature PD on the Alt-B pairset.				
Error_Delay_DS_A=	Time between overload shutdown and attempted new detection of a dual signature PD on the Alt-A pairset.				
Error_Delay_DS_B=	Time between overload shutdown and attempted new detection of a dual signature PD on the Alt-B pairset.				
Idle_Voff_SS_A=	Average voltage during the error delay period on the Alt-A pairset given a single signature PD		Voff	PSE75 PSE76	145.2.10.11
Idle_Voff_SS_B=	Average voltage during the error delay period on the Alt-B pairset given a single signature PD				
Idle_Voff_DS_A=	Average voltage during the error delay period on the Alt-A pairset given a dual signature PD				
Idle_Voff_DS_B=	Average voltage during the error delay period on the Alt-B pairset given a dual signature PD				

Uncovered PICS

PIC	Topic	Explanation
PSE23	Voltage exceeding 10V during connection check	Untestable - would require a PSE that produced connection check voltage exceeding 10V.
PSE59	Voltage Transient slew rates 3.5V/μsec	Not testable with PSA-3202 test blade. May generally be untestable if PSE voltage is not impacted substantially by load current transients.
PSE63	Reverse negative pair current with 3-pair powering	Requires hardware resource not available in all PSA-3202 test blades. May be addressed in future testing with Version 9 PSA-3202 blades.
PSE67	PSE contribution to Pair-to-Pair unbalance	Requires specialized hardware resource not available within PSA test blades.
PSE70	Inrush current sustained with port voltage beween 5V and 30V	Requires specialized hardware resource not available within PSA test blades.

PSE* PICS

Total	96
Covered	83
Future Coverage	6
Total Coverage	89
% Coverage	92.7%

PSE77	Current unbalance within a single pair up to 3%	Requires specialized hardware resource not available within PSA test blades.
PSE78	Impact of maximum single pair current unbalance to 100Base-Tx transmission	Requires specialized hardware resource not available within PSA test blades.
EL1 - EL20	LAN Interface Electrical Characteristics	Requires specialized fixturing, PSE port interventions, and specialized instrumentation to analyze electrical characteristics including differential LAN signals up to and exceeding 100MHz.
PSEEL1 - PSEEL26	LAN Interface Electrical Characteristics	Requires specialized fixturing, PSE port interventions, and specialized instrumentation to analyze electrical characteristics including differential LAN signals up to and exceeding 100MHz.

Other Coverages		
PSE1	Polarity configurations	Covered by standard test report
PSE24, PSE25, PSE26, PSE39, PSE54, PSE55	Autoclass PICS	To be addressed in future testing.